National Hybrid, Inc.

Mil-Std-1553/1760

NHI-1582 Enhanced Terminal

Bus Controller, Remote Terminal, Bus Monitor

User's Manual

Version 2.1
October 1997

The information provided in this document is believed to be accurate; however, no responsibility is assumed by NATIONAL HYBRIDINC. for its use, and no license or rights are granted by implication or otherwise in connection therewith. Specifications are subject to change without notice.

2200 Smithtown Avenue, Ronkonkoma, NY 11779
Telephone (516) 981-2400 Sales Fax 516-981-8888

Table of Contents

1.0.0 SCOPE
2.0.0 APPLICABLE DOCUMENTS
3.0.0 INTRODUCTION
3.1.0 FEATURES
3.1.1 GENERAL FEATURES
3.1.2 BUS CONTROLLER HIGHLIGHTS
3.1.3 REMOTE TERMINAL HIGHLIGHTS
3.1.4 BUS MONITOR HIGHLIGHTS
3.2.0 BLOCK DIAGRAM
3.3.0 PROTOCOL CHIP DESCRIPTION
3.3.1 HOST BUS INTERFACE UNIT
3.3.2 I/O BUS INTERFACE UNIT
3.3.3 INTERRUPT CONTROL UNIT
3.3.3.1 ICU REGISTERS
3.3.3.2 ICU FIFO
3.3.4 DUAL REDUNDANT FRONT END
3.3.4.1 MANCHESTER DECODER
3.3.4.2 MANCHESTER ENCODER
3.3.4.3 GAP COUNTER
3.3.4.4 RT - RT NO RESPONSE COUNTER
3.3.4.5 MINIMUM RESPONSE TIME COUNTER
3.3.4.6 FAIL -SAFE TIMEOUT COUNTER
3.3.5 MESSAGE PROCESSOR UNIT
3.4.0 RT HARDWIRE TERMINAL ADDRESS
4.0.0 DATA STRUCTURE
4.1.0 ADDRESS MAP
4.2.0 INTERNAL REGISTERS
4.2.1 CONTROL
4.2.2 POINTER TABLE ADDRESS
4.2.3 BASIC STATUS
4.2.4 INTERRUPT REQUEST
4.2.5 INTERRUPT MASK
4.2.6 INTERRUPT VECTOR
4.2.7 CONFIGURATION REGISTER 2
4.2.8 AUXILIARY VECTOR REGISTER
4.2.9 REAL-TIME CLOCK
4.2.10 RTC CONTROL REGISTER
4.2.11 FIFO READ
4.2.12 FIFO RESET
4.2.13 LAST COMMAND REGISTER
4.2.14 LAST STATUS REGISTER
4.2.15 RESET REMOTE TERMINAL
4.2.16 ENCODER STATUS
4.2.17 CONDITION REGISTER
4.2.18 ENCODER DATA REGISTER
4.2.19 ENCODER DATA TRANSMIT RQST
4.2.20 ENCODER COMMAND TRANSMIT REQUEST
4.2.21 EXTERNAL TERMINAL ADDRESS REGISTER

4.2.22 COMMAND OUTPUT PINS
4.2.23 I/O TAG WORD REGISTER
4.2.24 CONFIGURATION REGISTER 1
4.2.25 FRAME "A" POINTER
BLOCK "A" START
4.2.26 FRAME "A" LENGTH
BLOCK "A" END
4.2.27 FRAME "B" POINTER
BLOCK "B" START
4.2.28 FRAME "B" LENGTH
BLOCK "B" END
4.2.29 BC_FRAME_GAP
WORD_MONITOR_EOF_OPTIONS
4.2.30 CONFIGURATION REGISTER 3
4.2.31 MT ADDRESS FILTER (RT15-RT0)
4.2.32 MT ADDRESS FILTER (RT31-RT16)
4.2.33 BLOCK "A" LAST ADDRESS
4.2.34 BLOCK "B" LAST ADDRESS
4.3.0 RT DATA TABLES
4.3.1 MESSAGE ILLEGALITY
4.3.2 DATA TABLE TAG WORD
4.3.3 DATA TABLE POINTER
4.3.4 RT DATA TABLE BUFFERING SCHEME
4.3.4.1 RT RAM ACCESS
4.3.4.2 HOST RAM ACCESS
4.3.4.3 READ-MODIFY-WRITE
4.4.0 BC MESSAGE LISTS AND DATA TABLES
4.4.1 BC CONTROL WORD
4.4.2 BC COMMAND WORD
4.4.3 BC MESSAGE GAP WORD
4.4.4 BC TIME TAG MS WORD
4.4.5 BC TIME TAG LS WORD
4.4.6 BC DATA WORD
4.4.7 BC STATUS RESPONSE
4.4.8 BC MESSAGE TABLE FORMATS
4.5.0 MESSAGE MONITOR MESSAGE LISTS AND DATA TABLES
4.5.1 MESSAGE MONITOR TAG WORD
4.5.2 MESSAGE MONITOR COMMAND - STATUS WORD
4.5.3 MESSAGE MONITOR TIME TAG MS WORD
4.5.4 MESSAGE MONITOR TIME TAG LS WORD
4.5.5 MESSAGE MONITOR DATA WORDS
4.5.6 MESSAGE MONITOR MESSAGE TABLE FORMATS
4.6.0 WORD MONITOR DATA TABLES
4.6.1 WORD MONITOR TAG WORD
4.6.2 WORD MONITOR COMMAND - STATUS - DATA
4.6.3 WORD MONITOR TIME TAG MS WORD
4.6.4 WORD MONITOR TIME TAG LS WORD
5.0.0 RT MODE CODE OPERATION

Digitized by the Internet Archive
in 2024

https://archive.org/details/manualsplus_03676

5.1.0 GENERAL
5.2.0 TABLE OF MODE CODE RESPONSES
5.2.1 DYNAMIC BUS CONTROL (00000; T/R=1)
5.2.2 SYNCHRONIZE WITHOUT DATA (00001; T/R=1)
5.2.3 SYNCHRONIZE WITHOUT DATA (00001; T/R=1)
5.2.4 INITIATE SELF TEST (00011; T/R=1)
5.2.5 TRANSMITTER SHUTDOWN (00100; T/R=1)
5.2.6 OVERRIDE TRANSMITTER SHUTDOWN (00101; T/R=1)
5.2.7 INHIBIT TERMINAL FLAG (00110; T/R=1)
5.2.8 OVERRIDE INHIBIT TERMINAL FLAG (00111; T/R=1)
5.2.9 RESET REMOTE TERMINAL (01000; T/R=1)
5.2.10 RESERVED MODE CODES (01001-01111; T/R=1)
5.2.11 TRANSMIT VECTOR WORD (10000; T/R=1)
5.2.12 SYNCHRONIZE WITH DATA WORD (10001; T/R=0)
5.2.13 TRANSMIT LAST COMMAND (10010; T/R=1)
5.2.14 TRANSMIT BIT WORD (10011; T/R=1)
5.2.15 SELECTED TRANSMITTER SHUTDOWN (10100; T/R=0)
5.2.16 OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101; T/R=0)
5.2.17 RESERVED MODE CODES (10110-11111; T/R=1)
5.2.18 RESERVED MODE CODES (10110-11111; T/R=0)
6.0.0 INITIALIZATION
6.1.0 INTERNAL INITIALIZATION
6.2.0 HOST INITIALIZATION OF NHI-ET
7.0.0 INTERRUPT HANDLING
7.1.0 HARDWARE INTERRUPT ACKNOWLEDGE
7.2.0 SOFTWARE INTERRUPT ACKNOWLEDGE
8.0.0 TIPS - HINTS 'N TRICKS
8.1.0 BUS CONTROLLER APPLICATIONS
8.1.1 BC REGISTERS
8.1.1.1 CONFIGURATION REG 2
8.1.1.2 CONFIGURATION REG 1
8.1.1.3 FRAME "A" POINTER
8.1.1.4 FRAME "A" LENGTH
8.1.1.5 FRAME "B" POINTER
8.1.1.6 FRAME "B" LENGTH
8.1.1.7 CONDITION REGISTER
8.1.1.8 END OF FRAME GAP
8.1.1.9 CONFIGURATION REG 3
8.1.2 BC RAM
8.1.3 BC MESSAGE TABLE
8.1.4 BC CONTROL WORD
8.1.5 BC COMMAND WORD
8.1.6 MESSAGE GAP WORD
8.1.7 32 BIT TIME TAG(2 WORDS)
8.1.8 BC INTERRUPTS
8.1.9 BUS CONTROLLER EXAMPLES
8.1.10 SAMPLE BUS CONTROLLER MEMORY MAP
8.2.0 MESSAGE MONITOR APPLICATIONS
8.2.1 MESSAGE MONITOR REGISTERS

8.2.1.1 CONFIGURATION REG 2
8.2.1.2 CONFIGURATION REG 1
8.2.1.3 FRAME "A" POINTER
8.2.1.4 FRAME "A" LENGTH
8.2.1.5 FRAME "B" POINTER
8.2.1.6 FRAME "B" LENGTH
8.2.1.7 CONDITION REGISTER
8.2.1.8 CONFIGURATION REGISTER 3
8.2.1.9 ADDRESS FILTER (0-15)
8.2.1.10 ADDRESS FILTER (16-31)
8.2.2 MESSAGE MONITOR RAM
8.2.3 MESSAGE MONITOR MESSAGE TABLE
8.2.4 MESSAGE MONITOR TAG WORD
8.2.5 COMMAND WORD OR STATUS WORD
8.2.6 DATA WORD(S)
8.2.7 MESSAGE MONITOR EXAMPLE
8.3.0 WORD MONITOR APPLICATIONS
8.3.1 WORD MONITOR REGISTERS
8.3.1.1 CONFIGURATION REG 2
8.3.1.2 CONFIGURATION REG 1
8.3.1.3 BLOCK "A" START
8.3.1.4 BLOCK "A" END
8.3.1.5 BLOCK "B" START
8.3.1.6 BLOCK "B" END
8.3.1.7 CONDITION REGISTER
8.3.1.8 WORD MONITOR END OF BLOCK OPTIONS
8.3.1.9 CONFIGURATION REGISTER 3
8.3.2 WORD MONITOR EXAMPLE
8.4.0 SIMULTANEOUS MONITOR AND REMOTE TERMINAL
8.4.1 SIMULTANEOUS MODE INTERRUPT HANDLING
8.5.0 PC BOARD CONSIDERATIONS AND GUIDE LINES
9.0.0 PIN FUNCTIONAL DESCRIPTION
9.1.0 GENERAL PURPOSE SIGNALS
9.2.0 HOST INTERFACE IGNALS
9.3.0 DISCRETE I/O BUS INTERFACE SIGNALS
9.4.0 MIL-STD-1553B INTERFACE SIGNALS
10.0.0 ELECTRICAL CHARACTERISTICS
10.1.0 ABSOLUTE MAXIMUM RATINGS
10.2.0 OPERATING CONDITIONS
10.3.0 I/O TYPES & DESCRIPTIONS
10.4.0 I/O ELECTRICAL CHARACTERISTICS
11.0.0 TIMING DIAGRAMS
11.0.1 HOST WRITE CYCLE
11.0.2 HOST READ CYCLE
11.0.3 HOST READ-MODIFY-WRITE CYCLE
11.0.4 INTERRUPT ACKNOWLEDGE CYCLE
11.0.5 I/O WRITE CYCLE
11.0.6 COMMAND WRITE CYCLE

11.0.7 I/O READ CYCLE
11.0.8 TERMINAL ADDRESS READ CYCLE
11.0.9 TIMING DIAGRAM NOTES
11.1.0 TIMING PARAMETER TABLES
11.1.1 HOST READ, WRITE, and READ-MODIFY-WRITE TABLE
11.1.2 I/O READ and TERMINAL ADDRESS READ TABLE
11.1.3 I/O WRITE and COMMAND WRITE TABLE
11.1.4 INTERRUPT ACKNOWLEDGE CYCLE TABLE

12.0.0 PIN FUNCTIONS AND MECHANICAL DRAWINGS
12.0.1 NHI-1582ET- 69 PGA
12.0.2 NHI-1582ETFP- 68 QUAD FLAT PACK
12.0.3 NHI-1582ETGW- 68 QUAD GULL WING Lead Formed Flat Pack
14.0.0 APPLICATION NOTES
15.0.0 NHI-15182EMT(Extended Memory Terminal) ADDENDUM
15.0.1 EMT Features:
15.0.2 NHI-15182EMT 128 QFP Pin Functions
15.0.3 NHI-15182EMT 128 QFP Mechanical Drawing
16.0.0 MATING TRANSFORMER REFERENCE
17.0.0 ORDERING INFORMATION

1.0.0 SCOPE

This document defines the functional and electrical specification for National Hybrid's series of MIL-STD-1553B Enhanced Terminals (NHI-ET).

2.0.0 APPLICABLE DOCUMENTS

- MIL-STD-1553A
- MIL-STD-1553B Notices I and II
- MIL-STD-1760B
- MACAIR MDC A3818, A5690, A4905, A5332
- EFA/STANAG-3838 requirements for Eurofighter Aircraft

3.0.0 INTRODUCTION

The NHI-1582ET is a low cost complete Mil-Std-1553 Interface between a dual redundant MIL-STD-1553 bus and a host processor. The device functions as a programmable Bus Controller, Remote Terminal, and Bus Monitor containing a protocol chip, two +5V monolithic transceivers and 16K words SRAM. The unit is available packaged in a 1.1" x 1.1" 69 pin ceramic PGA, or 1.1" x 1.1" 68 pin ceramic quad flatpack. The only external components required are two coupling transformers.

The NHI-1582ET appears to the host computer as 16K words of 16 bit wide memory controlled by standard RAM signals. The device can thus be easily interfaced with all popular processors and buses. The built in interrupt controller supports an internal FIFO which retains header information for queuing up to 6 pending interrupt requests plus an overflow interrupt.

All modes of operation access data tables via pointers residing in RAM which facilitates multiple buffering. This allows buffers to change without moving data and promotes efficient use of RAM space. The data tables have programmable sizes and locations.

The NHI-1582ET is plug in compatible with the popular NHI-RT family of remote terminal with no changes to hardware or software required. The NHI-1582ET defaults to the NHI-RT remote terminal operation on power up.

3.1.0 FEATURES

The NHI-ET is form, fit, and function compatible to the NHI-RT series of parts. This interchange ability gives the user a high degree of flexibility when configuring a system around the NHI family of parts.

3.1.1 GENERAL FEATURES

- Single +5 volt supply.
- Operates from 10 Mhz clock.
- Contains two monolithic +5V transceivers
- Appears to host as a Dual Port Double Buffered 16K x 16 SRAM
- Low total power consumption.
- Footprint less than 1.25 square inches
- Ensures integrity of all shared data and control structures
- Built-in interrupt controller
- Internal FIFO is configurable to retain header information for queuing up to 6 pending interrupt requests plus an overflow interrupt, or as a 7 interrupt revolving FIFO
- Issues interrupts on any subset of T/R bit, subaddresses, mode commands, broadcast messages and errors.
- Provides interrupt priority input and output pins for daisy-chaining interrupt requests
- Contains a Timer Unit which provides 32 bit RTC (Real-Time-Clock) with 1, 2, 4, 8, 16, 32 and 64 uS internal, or user provided external clock resolution for data and event time tagging.
- Interfaces with an 8 bit discrete I/O bus
- Internally loops-back messages under host control for test purposes
- Selectable 768/672 us Failsafe Timer with complete Testability
- Low power CMOS technology

3.1.2 Bus Controller Highlights:

- Implements all Message Formats and Error Checking
- Simple setup and operation. Preset multiple pointer tables and message blocks. Only two Frame Pointer and Frame Length Registers are required to control unlimited number of message blocks
- BC initialized by writing to three Configuration Registers and the Interrupt Mask Register
- Executes lists of messages via Message Frame
- Configurable Local Retry and Interrupt Requests Enabled on Message by Message Basis
- Configurable Global Retry and Local Retry
- Programmable retries per message. None, Current Bus, Alternate Bus, Alternate Bus then Current Bus.
- Programmable response timeout of 14, 18, 26, or 42 microseconds.
- Programmable Intermessage Gap Time up to 4 mS with 1 uS resolution.
- Extended Intermessage Gap using NO-OP Feature.
- Programmable Frame Gap with 64 uS resolution.
- Programmable Interrupts for End of Message, End of Frame, Response Time Out, Message Error, Message Retry, RT Status Bit Set, and FIFO Overflow.
- Non-Maskable Bus Jam Interrupt.
- Host controlled commands to Start BC, Continuous Mode, Stop at End of Message, Stop at End of Frame, Abort, GOTO Alternate Frame.
- Dynamic Bus Switch Upon Successful Retry.

3.1.3 Remote Terminal Highlights:

- Dynamic Bus Control Acceptance
- DBCA_L bit is set in configuration register.
- Message Illegality is internally programmable. DOES NOT require external PROMS or glue logic.
- Employs data tables with individual tag words which indicate whether or not the data is valid, updated since last read, in the process of being updated, was received via broadcast command, or has been lost (i.e., updated more than once by a receive message before being read).
- Optionally sets the subsystem flag bit whenever stale data is transmitted or received data is overwritten.
- Issues interrupts to the host for any subset of subaddresses and mode commands.
- Stores interrupt vectors in a word deep FIFO.
- Built-in interrupt controller.
- Provides interrupt priority input and output pins for daisy-chaining interrupt requests.
- Includes a 32 bit real-time clock with programmable resolution for tagging receive, transmit, and mode code messages.
- Optionally resets the real-time clock in response to a "Synchronize" mode command.
- Optionally updates the lower 16 bits of the real-time clock in response to a "Synchronize With Data" command.
- Interfaces with an 8 bit discrete I/O bus.
- Indicates the reception of specific commands by outputting pulses on any one of 8 pins.
- Internally loops-back messages under host control for test purposes.
- Employs a decoder algorithm which ensures high noise immunity and a low error rate (word error rate typically less than 10^{-9} for 1553 noise test).
- Software RT Address Lockout.
- MDC3818 Status Response, Error Handling, Status Bit Definition, Mode Code Operation.
- Separate Broadcast Interrupts.

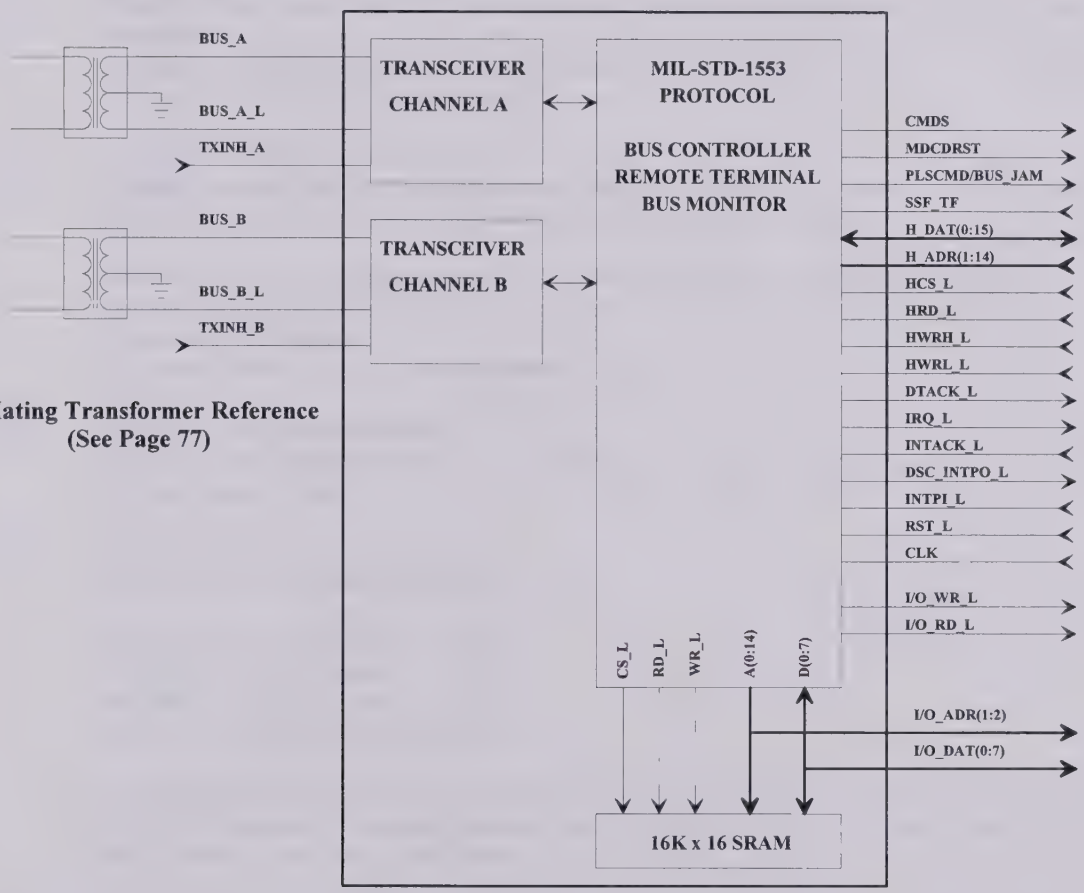
3.1.4 Bus Monitor Highlights:

- Simple setup and operation. Preset multiple data blocks. Only two MT Data Start Address and MT Data End Address Registers are required to control unlimited number of message blocks. The data block sizes and locations are totally programmable.
- MT initialized by writing to three MT Configuration Registers and the MT Interrupt Mask Register.
  - Error detection and reporting
- All encoding, timing and protocol errors defined by 1553B are detected.
- Programmable Monitor Modes:
  - Word Monitor, transfers all data with/without ID and Time Tag words.
  - Message Monitor, transfers all Command and Status words with/without ID and Time Tag ,
  - while data words are transferred directly to conserve memory space.
- Concurrent Bus Monitor and Remote Terminal operation.
- Selective Message Monitor, based on RT Address.
- Time-Tagging Message: Selectable 32 bit Real Time Clock with programmable tick rate.
- Programmable Interrupt for End of Block and End of Frame.

3.2.0 BLOCK DIAGRAM

The NHI-ETs contains two +5 volt transceivers, an ASIC, and a 32K x 8 SRAM. The ASIC performs all 1553 protocol functions, BUS CONTROLLER, BUS MONITOR and REMOTE TERMINAL. It controls accesses to the RAM such that it appears to the host CPU as 16K x 16 dual port memory. Although the RAM chip is only 8 bits wide, this is transparent to the user because the ASIC executes two fast RAM accesses for every 16 bit wide host access.

Since the NHI-ET appears to its host as RAM, no external logic is required when interfacing to the device. It is simply connected to the CPU's address bus, data bus, and control lines. There are NO EPROMS required to illegalize commands in the RT mode. Illegalization is performed internal to the protocol chip in the NHI-ET. The user sets up command illegalization when the NHI-ET is initialized. See sections on Message Illegalization and Host Initialization.



Mating Transformer Reference
(See Page 77)

NHI-1582ET ENHANCED TERMINAL FUNCTIONAL BLOCK DIAGRAM

The NHI-ET can be interfaced to an 8 bit data bus by folding the upper and lower bytes on top of each other and performing byte wide data transfers.

By default, the host has priority in accessing the I/O bus. When the host requests access to a device already in use by the protocol chip, the host *DTACK (*READY) signal is delayed by the NHI-ET. If either side (protocol chip or host) waits for access during the current cycle, it is automatically granted priority for the next cycle. The host can retain priority for successive cycles accessing the same address (this is required to guarantee the proper operation of host read-modify-write instructions - see pin *HCS for details) by keeping *HCS low.

3.3.0 PROTOCOL CHIP DESCRIPTION

The protocol chip contains the following modules:

I/O Bus Interface Unit	(IBIU)
Interrupt Controller Unit	(ICU)
Dual Redundant 1553 Front End	(DRFE)
Message Processor Unit	(MPU)

3.3.1 HOST BUS INTERFACE UNIT

The HBIU provides a standard RAM interface to the host bus. The module performs the following functions:

Provides NHI-ET device select and decodes host address to select registers.
Transfers data between the NHI-ET and the host (word and byte mode as well as read-modify-write are supported).
Provides priority input and output for daisy chaining host interrupts.
Outputs *DTACK signal indicating end of bus cycle.

3.3.2 I/O BUS INTERFACE UNIT

The IBIU controls the RAM and I/O residing on the I/O bus so that it appears to the host as a pseudo dual port RAM (i.e., shared memory). The unit implements the following functions:

Arbitrates between host and protocol chip initiated accesses to the RAM and host data bus.
Decodes address lines to select device (e.g. RAM, external byte-wide I/O, external terminal address buffer, command output register).
Generates control signals to access the selected device.

3.3.3 INTERRUPT CONTROL UNIT

The ICU is an 8 input vectored interrupt controller. It contains eight registers as well as a FIFO for storing pending interrupt vectors.

3.3.3.1 ICU REGISTERS

The ICU contains the following registers

INTERRUPT REQUEST register	(IRR)
INTERRUPT MASK register	(IMR)
INTERRUPT VECTOR register	(IVR)
AUXILIARY VECTOR register	(AVR)

The INTERRUPT REQUEST register samples 8 inputs originating from internal modules. Since the host can write to this register, all interrupt sequences can be software driven for program debugging. The inputs and their priorities (level 7 has highest priority) are as follows:

PRIORITY	RT INTERRUPT	BC INTERRUPT	MT INTERRUPT
0	VALID TX/RX EOM	END of MESSAGE	N/A
1	INVALID TX/RX EOM	END of FRAME	NA
2	VALID MODE CODE EOM	ERROR	N/A
3	INVALID MODE CODE EOM	RETRY	N/A
4	FIFO OVERFLOW	FIFO OVERFLOW	N/A
5	VALID BROADCAST	STATUS SET	END OF FRAME
6	INVALID BROADCAST	NO RESPONSE	N/A
7	FAIL SAFE TIMEOUT	FAIL SAFE TIMEOUT	N/A

Note: RT Interrupts 5 & 6 are enabled only when separate Broadcast Tables are used.

As soon as an interrupt is requested, its vector is pushed onto the FIFO - so the chronological order of the requests normally determines the order in which they will be serviced. Simultaneous requests, however, are pushed onto the FIFO according to the priority of the pending interrupts.

The INTERRUPT MASK register masks the corresponding inputs to the INTERRUPT REQUEST register.

The INTERRUPT VECTOR register holds the 3 bit interrupt priority level and an additional 5 bit field (see paragraph on INTERRUPT VECTOR register for details).

The AUXILIARY VECTOR register contains an additional byte of information related to the interrupt request (see paragraph on AUXILIARY VECTOR register for details).

3.3.3.2 ICU FIFO

The ICU FIFO is 16 bits wide and 7 words deep. Whenever an unmasked interrupt request is issued by the message processor, a word is pushed onto the FIFO. When an interrupt is acknowledged by the host, a word is popped from the FIFO and used to update the IVR and the AVR.

The host can read the FIFO by simply popping its contents. This is done by reading the FIFO located at address 8 (refer to address map). The interrupt request output, *IRQ, will go inactive after the FIFO is emptied in this way.

The host can mask the *IRQ output by resetting the INTERRUPT REQUEST ENABLE bit in the CONTROL register; however this does not prevent the device from pushing interrupt requests onto the FIFO.

If an interrupt request occurs when the FIFO is full, a vector indicating FIFO overflow is first pushed onto the FIFO and then the vector which caused the overflow is pushed onto the FIFO. As a result, the 2 oldest vectors are lost. All further pushes are then inhibited until the host pops the vector indicating the overflow.

The above mechanism ensures that the host will always be notified of FIFO overflows and will always obtain the 2 interrupt vectors immediately preceding the overflow condition.

If interrupt 4 is masked, the FIFO operates in the revolving mode; vectors are continuously pushed onto the FIFO. After the 7th vector is pushed without any pops, each additional vector pushed causes the oldest vector to be lost.

The FIFO can be emptied by writing (any value) to address 8 (in words).

3.3.4 DUAL REDUNDANT FRONT END

The DRFE performs serial to parallel and parallel to serial conversion as well as basic format and timing validation. The unit contains the following:

Manchester encoders/decoders
Gap counter
No response counter
Minimum response time counter
Timeout counter

3.3.4.1 MANCHESTER DECODER

The decoder translates serial Manchester bi-phase signals to 16-bit words and outputs the following signals:

Valid command word received
Valid data word received
Invalid word received (parity, incorrect bit count, invalid Manchester encoding, gap)
Broadcast command received
Begin new message (i.e., end of a valid legal command for this Remote Terminal)

3.3.4.2 MANCHESTER ENCODER

The encoder receives 16 bit words and transmits them with the appropriate sync and parity as a serial Manchester bi-phase signal. The outputs of the encoder can be loop-backed into either decoder for test purposes.

3.3.4.3 GAP COUNTER

The gap counter checks contiguity of successive words. If the time between "contiguous" words (measured from zero-cross of parity to zero-cross of sync) exceeds 3.5 - 3.7 microseconds, the message is invalidated.

3.3.4.4 RT - RT NO RESPONSE COUNTER

The no response counter checks the response time of the transmitting RT in a RT to RT transfer. If the response time is exceeded, the message is invalidated. The response time is software programmable (14, 18, 26, 42 microseconds) to accommodate systems with long cables and/or slow terminals.

3.3.4.5 MINIMUM RESPONSE TIME COUNTER

The minimum response time counter ensures that the response will be no sooner than 4 microseconds (measured from zero-cross of parity to zero-cross of sync).

3.3.4.6 FAIL -SAFE TIMEOUT COUNTER

This counter inhibits the encoder outputs and issues a TIMEOUT interrupt whenever continuous transmission exceeds 768/672 microseconds. Transmission will remain inhibited until a command is received on the same bus or the part is reset.

3.3.5 MESSAGE PROCESSOR UNIT

The MPU forms the heart of the protocol chip and controls the operation of the Dual Decoder, Encoder, and Interrupt Controller. This unit is activated by the reception of a valid legal command addressed to the RT in the RT mode and the START bit in CONFIGURATION 1 in both the BC and MT modes.

The MPU performs the following functions:

Recognizes the various message types (for BC, MT, and RT) and responds with the appropriate sequence of control signals.
Validates format and timing of received data words.
Checks command legality.
Responds with status/data.
Calculates all data bus addresses for accessing the RAM and discrete I/O.
Updates RAM data table contents, including tag words.
Optionally time tags data tables.
Issues interrupt requests to the ICU.

The maximum response time of the NHI-ET in the RT mode is less than 6.0 microseconds (measured from zero-cross to zero-cross).

3.4 RT HARDWIRE TERMINAL ADDRESS

The terminal address of the NHI-ET can be hardwired using I/O DAT(5:0). I/O DAT(4:0) are used for the terminal address, I/O DAT0 being the LSB, and I/O DAT5 is used to set odd parity in the address. These pins CANNOT be directly connected to +5 or ground since the I/O data bus drives the NHI-ET's internal RAM. The address must be wired using pull-up and pull-down resistors. There are 64K internal pull-up resistors in the protocol chip, so only external pull-down resistors of 4.7K are required. The Hardwire Address is read and loaded into the terminal at Power-On Reset, Hardware Reset, and Software Reset.

The terminal address can be changed at any time through software by writing a new address to the Basic Status Register, however, if any of the above resets occur, the Hardwire Address will be re-loaded into the terminal. The software address can be locked out by setting Bit2 in Configuration Register 1.

4.0.0 DATA STRUCTURE

4.1.0 ADDRESS MAP

The NHI-ET appears to the host as 16K words of memory divided into the following blocks:

Address Range	Description
0 - 29	Internal Control and Status registers
30	External RT address / Command output pins
31	I/O tag word
32 - 35	I/O space (accessed on the Discrete I/O bus)
64 - 16383	Shared RAM (accessed on the Host I/O bus)

The following address map table defines all addresses relevant to the user.

ADDRESS	CONTENTS/OPERATION	R/W
0	CONTROL REGISTER	R/W
1	POINTER TABLE ADDRESS REGISTER	R/W
2	BASIC STATUS REGISTER	R/W
3	IMR (lower byte)	R/W
3	IVR (upper byte)	R
3	IRR (upper byte)	W
4	IVR (lower byte)	R/W
4	AVR (upper byte)	R
4	CONFIGURATION REGISTER 2(Upper Byte, BT/MT Only)	W
5	RTC_HIGH	R
6	RTC_LOW	R
7	RTC CONTROL REGISTER	R/W
8	FIFO READ	R
8	FIFO RESET (both bytes)	W
9	CONFIGURATION REGISTER 1	R/W
10	***RESERVED***	
11	LAST COMMAND REGISTER	R
12	LAST STATUS REGISTER	R
13	FRAME "A" (Msg List Addr)/ BLOCK "A" START ADDR	R/W
14	FRAME "A" LENGTH (Msg List Len) / BLOCK "A" END ADDR	R/W
15	RESET RT (both bytes)	W
16	FRAME "B" (Msg List Addr) / BLOCK "B" START ADDR	R/W
17	RAME "B" LENGTH / BLOCK "B" END	R/W
18	ENCODER STATUS REGISTER	R
19	CONDITION REGISTER	R
20	BC FRAME GAP / WORD MONITOR END OF FRAME OPTIONS	R/W
21	CONFIGURATION REGISTER 3	R/W
22	MESSAGE MONITOR ADDRESS FILTER 1 (0 - 15)	R/W

23	ENCODER DATA REGISTER *	R/W
24	ENCODER DATA TX REQUEST (both bytes)*	W
25	ENCODER CMD TX REQUEST (both bytes) *	W
26	MESSAGE MONITOR ADDRESS FILTER 2 (16 - 31)	R/W
27	WORD MONITOR LAST ADDRESS BLOCK "A"	R
28	WORD MONITOR LAST ADDRESS BLOCK "B"	R
29	***RESERVED***	
30	EXTERNAL RT ADR BUFFER (lower byte)	R
30	COMMAND OUTPUT PINS	W
31	I/O TAG REGISTER	R/W

*In order to write to addresses 23, 24, or 25, the ET must be in loop-back in the RT mode (see CONTROL register for details).

4.2.0 INTERNAL REGISTERS

4.2.1 CONTROL Address: 0 R/W BC/MT/RT

This register controls the general operation of the NHI-ET.

15	14	13	12	11	10	9	8
HWD	RSP1	RSP0	TSTFST	NBCST	TXINH	LOOPB	LOOPA
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
IRE	MIO	CMDO	SRQRST	SSF_TF	NTAG	BINH	AINH

HWD **Bits: 15** **BC/RT**

HWD=1 enables high word detection.

This option allows words to be invalidated when bus activity is detected instead of a gap (e.g.: extra bits/words following a transmit command or the last data word in a receive message).

RSP1, RSP0 **Bits: 14,13** **BC/RT**

These bits define the response timeout for RT-RT messages in the RT mode and terminal response in the BC mode as follows:

RSP1	RSP0	Timeout (uS)
0	0	14
0	1	18
1	0	26
1	1	42

TSTFST **Bits: 12** **RT**

TSTFST = 1 enables testing of the FAIL SAFE time out.

When this feature is enabled, the RT will transmit continuously once it is enabled by a valid message. The encoder will be inhibited after 768/674us. It will be enabled by a reset or the reception of another valid message. If this bit is set to 0 during an RT transmission, before the required number of words have been transmitted, the encoder will return to normal operation and stop at the proper message length.. If it is set to 0 after the message length has been exceeded, the current word will be completed and normal operation resumed. This feature can be used in the LOOPBACK mode to automatically transmit data words.

The RT encoder will remain in the tester mode until the CPU sets this bit to 0.

The TSTFST Bit Must Always Be Set to Zero During Normal Operation!!!

NBCST **Bits: 11** **RT**

NBCST=1 specifies that broadcast commands should be ignored by the RT.

TXINH **Bits: 10** **BC/RT**

TXINH=1 inhibits transmission by forcing TXA=TXAN=0 and TXB=TXBN=0.

LOOPA(B) **Bits: 9, 8** **RT**

LOOPA(B)=1 defines that decoder A (B) inputs shall be connected internally to the encoder outputs rather than the 1553 transceiver for test purposes.

IRE **Bits: 7** **BC/MT/RT**

IRE=1 enables the interrupt request output, *IRQ.
IRE=0 disables all interrupt requests; however, interrupt vectors are still pushed onto the FIFO.

MIO **Bits: 6** **RT**

MIO=1 defines that certain reserved mode commands with data shall be legal and access the I/O bus without dependence on host initialization or the BUSY bit in the BASIC STATUS register. This feature can be used, for example, to set a watchdog timer or read a hardware status register via the 1553 bus even though the host's state may be undefined.

The I/O operations are restricted to the data word's lower byte. The mode commands and their corresponding I/O addresses are as follows:

T/R	MODE CODE (Decimal)	I/O ADR(2,1)	*I/O WR	*I/O RD
T	24	00	1	0
T	25	10	1	0
R	27	10	0	1
R	28	00	0	1

CMD0 **Bits: 5** **RT**

CMD0=0 Specifies that after a legal valid command is received, a pulse shall be outputted on a pin specified by the PULSE field in the corresponding data table tag word. The pulse is activated together with 2 I/O control signals (CMDS=1 and *I/O WR = 0).

CMD0=1 Specifies that after a valid legal command is received, the word count/mode code field (together with CMDS=1 and *I/O WR = 0) shall be outputted on the 5 least significant bits of the discrete I/O bus. (Although the protocol chip outputs the entire command, only 5 bits are outputted by the NHI-RT due to pin-out restrictions).

SRQRST **Bits: 4** **RT**

SRQRST=1 specifies that the service request bit in the STATUS register will be reset upon reception of a valid "Transmit Vector Word" mode command.

SSF_TF **Bits: 3** **RT**

SSF_TF=0 specifies that the sub-system flag in the 1553 status word will be determined by the value of the SSF_TF pin.

SSF_TF=1 specifies that the terminal flag in the 1553 status word will be determined by the value of the SSF_TF pin.

NTAG **Bits: 2** **RT**

NTAG=1 specifies that all the data tables shall be without tag words. This mode of operation can be used to store received data from several subaddresses into a contiguous block without interspersed tag words. This feature can facilitate, for example, software upload.

BINH **Bits: 1** **BC/RT**

BINH=1 disables reception on bus B.

AINH **Bits: 0** **BC/RT**

AINH=1 disables reception on bus A.

4.2.2 POINTER TABLE ADDRESS Address: 1 R/W RT

This register holds the address of the table of pointers used in the RT mode when accessing data tables. The address is specified as a word address in the lower 4K of the memory space. After POR the register is initialized with the value 1000 (hex).

Note: The RT pointer table must always be located in the lower 4K words of memory.

4.2.3 BASIC STATUS Address: 2 R/W RT

This register defines the terminal address as well as default values for all status bits. The 1553 status word is OR'ed with this register before transmission. The bits in the BASIC STATUS register correspond to the bits in the STATUS register and their function is defined in MIL-STD-1553B.

15	14	13	12	11	10	9	8
TADR4	TADR3	TADR2	TADR1	TADR0	ME	INSTR	SREQ
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD	RSVD	RSVD	BCR	BUSY	SSF	DBCA	TF

The mechanism employed by the protocol chip for initializing the terminal address is designed to avoid dedicated pins. Upon POR the terminal address and its parity are automatically read from address 30 on the I/O bus. The value can be supplied in 2 ways: by enabling the output of an external terminal address buffer or by employing pull-up/down resistors to define a default value for the 6 least significant bits of the I/O data bus. Odd parity is used to define a valid terminal address; even parity will inhibit reception on both buses. After POR, the host can change the terminal address through software by writing to the TADR field with any desired value. In addition, this operation will enable reception. Providing Bit 2 of Configuration Register is set to "0".

The host can check the validity of the parity bit obtained from the I/O bus by reading address 30; if the most significant bit in the lower byte equals 1, the parity is invalid.

If the TADR is not defined externally (by pull-down resistors or a buffer), there is no danger of a false response before host initialization because internal pull-up resistors on the I/O bus guarantee an incorrect terminal address parity.

When BUSY=1, 1553 message accesses to the RAM are inhibited, however the RT will respond with status

as required by MIL-STD-1553B. The mode commands "Transmit Status Word", "Transmit Last Command Word", "Reset Remote Terminal", "Transmitter Shutdown", "Override Transmitter Shutdown" and the reserved mode commands legalized by MIO (see the CONTROL register for details) are not affected by BUSY. In addition, all output pulses issued after valid command reception are inhibited when BUSY=1 (except for the signal MDCDRST which is pulsed after receiving the mode command "Reset").

After POR(MRST), BUSY is set to "1"; this prevents the RT from using undefined pointers before the host has had a chance to initialize the POINTER TABLE. The default value for all other status bits is "0" and the TADR field is loaded with the hardwired address.

The BUSY Bit in the LAST STATUS REGISTER is cleared on receipt of the first command after a RESET, except if that command is TRANSMIT LAST STATUS or TRANSMIT LAST COMMAND mode command.

The BUSY Bit in the LAST STATUS REGISTER can be cleared by bit using BIT 6 in the RTC CONTROL REGISTER. See RTC CONTROL REGISTER for details.

4.2.4 INTERRUPT REQUEST

Address: 3 Ubyte W BC/MT/RT

The INTERRUPT REQUEST register holds 8 types of interrupt requests (see section on INTERRUPT CONTROL UNIT for details). Interrupt requests are active high and upon POR the register is cleared (see initialization section).

7	6	5	4	3	2	1	0
IREQ7	IREQ6	IREQ5	IREQ4	IREQ3	IREQ2	IREQ1	IREQ0

4.2.5 INTERRUPT MASK

Address: 3 Lbyte R/W BC/MT/RT

The INTERRUPT MASK register masks the corresponding inputs to the INTERRUPT REQUEST register; the bits mask when high. Upon POR, all interrupts are masked (see initialization section).

7	6	5	4	3	2	1	0
IMSK7	IMSK6	IMSK5	IMSK4	IMSK3	IMSK2	IMSK1	IMSK0

4.2.6 INTERRUPT VECTOR

Address: 3 Ubyte R BC/MT/RT

Address: 4 Lbyte R/W BC/MT/RT

The IVR is read only in the upper byte at address 3 and is read/write in the lower byte at address 4. It contains interrupt header information which is popped off the FIFO. CNFG_2 is write only in the upper byte at address 4 and is used for operational control of the part.

Addr 3(4)	15(7)	14(6)	13(5)	12(4)	11(3)	10(2)	9(1)	8(0)
RT(BC/MT)	D_4(CNT_4)	D_3(CNT_3)	D_2(CNT_2)	D_1(CNT_1)	D_0(CNT_0)	L_2	L_1	L_0

L(2:0)

The INTERRUPT VECTOR register holds the interrupt priority (LLL) determined by the message processor and a host programmable 5 bit displacement which is a function of the BC, MT and RT modes of operation. The LLL field is popped from the FIFO and latched into the IVR during the interrupt acknowledge cycle or whenever the FIFO is popped by a host read instruction. Upon POR, this register is undefined.

D(4:0)

In the RT mode the DDDDD field is inputted by the CPU. This is used as an offset for the interrupt vector.

CNT(4:0)

In the BC and MESSAGE MONITOR modes the CNT field is the lower five bits of the number of the message in the frame which caused the interrupt. This data is popped from the FIFO by the BC/MT.

4.2.7 CONFIGURATION REGISTER 2 Address: 4 Ubyte W BC/MT/RT

15	14	13	12	11	10	9	8
GO_DEF FRAME	ABORT	STOP_END0F FRAME	STOP_ENDOF MSG	CLR_DISCFLG	GO_EOF_ CNTNU	GO_NEXT MSG	DO_EOM & CNTNU

NOTE: Bits 8 -10 are only used in the BC mode during a BUS JAM condition.

GO_DEF_FRAME **Bits: 15** **BC/MT**

When a "1" is written to this bit, the DEFAULT FRAME, defined by bit 12 in CONFIGURATION REGISTER 1, is made the active frame.

ABORT **Bits: 14** **BC/MT**

When a "1" is written to this bit, all BC and MT processing is terminated and the NHI-ET goes off-line. The BC or the MT must be re-started to again become active.

STOP_END OF FRAME **Bits: 13** **BC/MT**

When a "1" is written to this bit, the BC or the MT will go off-line after the last message in the frame or block has been processed. The BC or the MT must be re-started to again become active.

STOP_END OF MESSAGE **Bits: 12** **BC/MT**

When a "1" is written to this bit, the BC or the MT will go off-line after the current message in the frame or block has been processed. The BC or the MT must be re-started to again become active.

CLR_DISC FLAG **Bits: 11** **RT**

When a "1" is written to this bit, the 1760 DISCONNECT FLAG is cleared. This flag indicates that a store has been released and all the address bits and the parity bit on the hardwire address are "1's". The flag is read on the IPO_DSC pin and bit 6 of the EXTERNAL TERMINAL ADDRESS REGISTER.

GO_EOF & CONTINUE **Bits: 10** **BC**

When a "1" is written to this bit after a BUS JAM condition has halted the BC operation, the BC will ignore all further messages in the current frame, proceed to the end of the frame and perform the programmed EOF operations.

GO_NEXT MESSAGE **Bits: 9** **BC**

When a "1" is written to this bit after a BUS JAM condition has halted the BC operation, the BC will abort the current message and NOT perform the programmed EOM operations; instead, the next message in the frame will be activated. If there are no more messages in the frame, the programmed EOF operations will be performed.

DO_EOM & CONTINUE **Bits: 8** **BC**

When a "1" is written to this bit after a BUS JAM condition has halted the BC operation, the BC will perform the programmed EOM operations, then the next message in the frame will be activated. If there are no more messages in the frame, the programmed EOF operations will be performed.

The contents of CONFIGURATION REGISTER 2 are not affected by these operations and all the bits are always read by the host as "0" after the indicated action has been completed.

4.2.8 AUXILIARY VECTOR REGISTER Address: 4 Ubyte R BC/MT/RT

This register contains additional information related to the interrupt request. The upper 7 bits are popped from the FIFO and latched into the AVR during the interrupt acknowledge cycle or whenever the FIFO is popped by a host read instruction to address 8. Upon POR, this register is undefined.

MODE	15	14	13	12	11	10	9	8
RT	EMP	BUS	T/R	SADR4 MODE4	SADR3 MODE3	SADR2 MODE2	SADR1 MODE1	SADR0 MODE0
BC	EMP	BUS	FRAME	CNT 9	CNT 8	CNT 7	CNT 6	CNT 5
MT	EMP	BUS	FRAME	CNT 9	CNT 8	CNT 7	CNT 6	CNT 5

EMP
EMP=1

BUS
BUS=0 (1) Indicates that the message was on bus A (B).

T/R
T/R=0 (1) indicates a receive (transmit) message.

SADR / MODE
This field defines the sub-address or mode code.
Note: the interrupt level distinguishes between regular transmit/receive commands and mode commands.

CNT
In the BC and MESSAGE MONITOR modes the CNT field is the upper five bits of the number of the message in the frame which caused the interrupt.

FRAME
In the BC and MESSAGE MONITOR modes this field the frame which caused the interrupt.
FRAME = 0 (1) indicates frame A (B).

4.2.9 REAL-TIME CLOCK

The RTC is a 32 bit up-counter which can be used for time- tagging in the BC, MT and RT modes. If the time-tagging option is in effect, the RTC is sampled and stored in 2 words in the data table The most significant word is stored first.

When messages are time-tagged in the RT mode, the host should not write data to the first 2 locations following the data table tag word since they will be overwritten with the value of the RTC.

In the RT mode, the RTC can be reset by the mode command "Synchronize Without Data" and the least significant 16 bits can be updated by "Synchronize With Data". The full 32 bits can be updated using the first two data words in a receive command. See RTC CONTROL REGISTER for details.

The RTC can be read and reset by the host at any time. Since the RTC consists of 32 bits, at least 2 memory cycles are required to read all of its value. As a result, a carry-out from the lower word can occur between the read cycles. A mechanism is therefore provided to solve this potential difficulty.

If the host reads the RTC as two 16 bit words, *LOCK should be initialized to 1 in the RTC CONTROL register. In this case, when the host reads the upper word, all 32 bits are latched into the host output register. The value in the output register remains unchanged until the host finishes reading the lower word of the RTC.

If the host reads the RTC in bytes, *LOCK should be initialized to 0. In this case, when the host reads any of the bytes of the RTC, all 32 bits are latched into the host output register and its value remains unchanged

until updating is re-enabled by reading the RTC CONTROL register. The RTC resolution can be programmed equal to 1, 2, 4, 8, 16, 32, or 64 microseconds.

4.2.10 RTC CONTROL REGISTER — Address: 7 — R/W — BC/MT/RT

The RTC is controlled by the RTC CONTROL register which has the following format:

15	14	13	12	11	10	9	8
RTCRST	RST_LAST	RES2	SYNUPD	*LOCK	SYNRST	RES1	RES0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
M1760	BUSY_OPT	RST_BUSY	PRESET4	PRESET3	PRESET2	PRESET1	PRESET0

RTCRST — **Bits: 15** — **BC/MT/RT**

When a "1" is written to RTCRST, a reset pulse is issued to the RTC. The contents of the register are not affected by this operation and RTCRST is always read by the host as "0".

RST_LAST — **Bits: 14** — **BC/MT/RT**

When a "1" is written to RST_LAST, all the bits in the LAST STATUS REGISTER except the ADDRESS field and the BUSY bit are set to a "0". The contents of the register are not affected by this operation and RST_LASTis always read by the host as "0".

RES2 — **Bits: 13** — **BC/MT/RT**

See RTC Resolution Table.

SYNUPD — **Bits: 12** — **RT**

SYNUPD=1 specifies that the lower 16 bits of the RTC will be updated whenever a valid mode command "Synchronize With Data" is received by the ET.

***LOCK** — **Bits: 11** — **RT**

0 = enables updating of the host output register after the RTC CONTROL register is read (this feature is needed to support byte wide read cycles).

1 = enables updating of the host output register after the lower RTC word is read.

SYNRST — **Bits: 10** — **BC/MT/RT**

SYNRST=1 specifies that the RTC shall be reset whenever a valid mode command "Synchronize Without Data" is received by the ET.

RES — **Bits: 13, 9, 8** — **BC/MT/RT**

This field defines the resolution of the RTC in microseconds as follows:

RTC RESOLUTION TABLE

Resolution (us)	13	9	8
1	0	0	0
2	0	0	1
4	0	1	0
8	0	1	1
16	1	0	0
32	1	0	1

64	1	1	0
OFF/EXT	1	1	1

Note: Some NHI-ET device type have an external TIME TAG CLOCK input.

M1760 **Bits: 7** **RT**

M1760=1specifies that the RT shall comply with MIL-STD-1760A. This mode of operation has 2 consequences: first, the mode command "Synchronize With Data" updates the lower 16 bits of the RTC only if the least significant data bit is "0" and second, the IPO_DSC pin serves as a store disconnect signal rather than an interrupt priority output.

BUSY _OPT **Bits: 6** **RT**

0 = MRST, Software Reset and MODE CODE_08 RESET will set the BUSY bit in the LAST STATUS REGISTER and the BASIC STATUS REGISTER to a "1".

1 = Only MRST will set the BUSY bit in the LAST STATUS REGISTER and the BASIC STATUS REGISTER to a "1".

RST_BUSY **Bits: 5** **RT**

When a "1" is written to RST_BUSY, the BUSY bit in the LAST STATUS REGISTER is set to a "0". The contents of the register are not affected by this operation and RST_BUSY is always read by the host as "0".

PRESET **Bits: 4, 3, 2, 1, 0** **RT**

These bits provide a method to perform a double word(32 bit) preset to the RTC. When this bit field is set to any number from 1 to 30(bit 0 = LSB), the first two words of a receive message whose subaddress is equal to this value will be used to preset the internal RTC. The most significant word is received first. If this field is equal to a "0" or "31", the RTC will not be preset. All bits in this register are cleared during initialization of the ET.

4.2.11 FIFO READ — Address: 8 — R — BC/MT/RT

This address is used to read the contents of the interrupt FIFO. Reading this address pops the FIFO and updates the IVR and the AVR.

4.2.12 FIFO RESET — Address: 8 — W — BC/MT/RT

Writing any value to this address empties the FIFO.

4.2.13 LAST COMMAND REGISTER — Address: 11 — R — RT

This register holds the last command word as defined by MIL-STD-1553B. The contents are not defined after initialization of the RT.

4.2.14 LAST STATUS REGISTER — Address: 12 — R — RT

This register holds the last status word as defined by MIL-STD-1553B. After initialization of tEe RT, the BUSY bit=1, the TADR field contains the hardwire address, and all other bits are set to 0. See RTC CONTROL REGISTER for special options.

4.2.15 RESET REMOTE TERMINAL — Address: 15 — W — BC/MT/RT

Writing a word to address 15 resets the RT and causes it to perform its initialization (see initialization section).

4.2.16 ENCODER STATUS Address: 18 R BC/RT

This register contains flags indicating the status of the encoder. These flags are intended to facilitate transmission of messages in loop-back mode during self-test.

15	14	13	12	11	10	9	8
TXREQ_L	X	X	X	X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
EOTX_L	X	X	X	X	X	X	FAILSAFE_L

TXREQ_L **Bits: 15** **RT**

TXREQ_L = 0 indicates that the encoder is ready to accept the next word for transmission. This bit should equal "0" before loading the encoder with the next word. In order to transmit contiguous words, the next word should be loaded within 18 microseconds after *TXREQ transitions to "0".

EOTX_L **Bits: 7** **RT**

EOTX = 0 indicates that the encoder has completed transmission and that there are no pending requests.

FAILSAFE_L **Bits: 0** **BC/RT**

FAILSAFE_L = 0 FAILSAFE TIME OUT has occurred. This bit will be set to a "1" when a new message is received or during a reset.

4.2.17 CONDITION REGISTER Address: 19 R BC/MT/RT

This register contains information about the command being processed by the NHI-RT. It also reports if the terminal flag is enabled and if the transmitters for bus "A" and bus "B" are enabled.

15	14	13	12	11	10	9	8
X	X	AXEN	BXEN	TFE	X	MDCD_L	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
X	CUFRBSY	EOF_B	EOF_A	CUR_FRM	CUR_BUS	BUSJAM_B	BUSJAM_A

X = NOT USED

AXEN **Bits: 13** **BC/RT**

AXEN = 1 indicates that transmitter A is enabled. This bit is set to a "1": at POWER UP, if the NHI-RT is RESET, after receipt of a "Reset" mode code, or after receipt of an OVERRIDE TRANSMITTER SHUTDOWN mode code on the B bus.

AXEN = 0 indicates that transmitter A is inhibited. This bit is set to a "0" after receipt of TRANSMITTER SHUTDOWN mode code on the B bus.

BXEN **Bits: 12** **BC/RT**

BXEN = 1 indicates that transmitter B is enabled. This bit is set to a "1": at POWER UP, if the NHI-RT is RESET, after receipt of a "Reset" mode code, or after receipt of an OVERRIDE TRANSMITTER SHUTDOWN mode code on the A bus.

BXEN = 0 indicates that transmitter B is inhibited. This bit is set to a "0" after receipt of a TRANSMITTER SHUTDOWN mode code on the A bus.

TFE **Bits: 11** **RT**

TFE = 1 indicates that the TERMINAL FLAG bit in the status word can be set to a "1" . This can be done in the BASIC STATUS REGISTER or by the TERMINAL FLAG pin on the NHI-ET. This bit is set to a "1" at POWER UP, if the NHI-RT is RESET, after receipt of a RESET MODE CODE, or after receipt of an OVERRIDE INHIBIT TERMINAL FLAG mode code.

TFE = 0 indicates that the TERMINAL FLAG bit in the status word CANNOT be set to a "1". This bit is set to a "0" after receipt of an INHIBIT TERMINAL FLAG mode code.

MDCD_L **Bits: 9** **RT**

MDCD_L = 1 indicates that the last command received was NOT a mode code.
MDCD_L = 0 This bit is set to a "0" when a mode code is received.

CUFRBSY **Bits: 6** **BC/MT**

1 = The current frame of data block is busy. It is active and could be receiving or transmitting data.

EOF_B **Bits: 5** **BC/MT**

1 = Frame "B" or data block "B" has finished processing data and in now inactive.

EOF_A **Bits: 4** **BC/MT**

1 = Frame "A" or data block "A" has finished processing data and in now inactive.

CUR_FRM **Bits: 3** **BC/MT**

0 = Frame "A" or block "A" is the current active frame of block.
1 = Frame "B" or block "B" is the current active frame of block.

CUR_BUS **Bits: 2** **BC/MT**

0 = Bus "A".
1 = Bus "B".

BUSJAM_B **Bits: 1** **BC**

1 = Bus "B" has been jammed by continuous transmission from an RT. This condition is indicated when an RT transmits more extra words then the value set in CONFIGURATION REGISTER 3 (See CONFIG REG 3 for details).

BUSJAM_A **Bits: 0** **BC**

1 = Bus "A" has been jammed by continuous transmission from an RT. This condition is indicated when an RT transmits more extra words then the value set in CONFIGURATION REGISTER 3 (See CONFIG REG 3 for details).

4.2.18 ENCODER DATA REGISTER Address: 23 R/W RT

This register contains data to be transmitted when performing a loop back test.

4.2.19 ENCODER DATA TRANSMIT RQST Address: 24 W RT

Writing (any value) to this address causes the contents of the ENCODER DATA REGISTER to be sent as a data word. This instruction together with the ENCODER COMMAND TRANSMIT REQUEST can be used to loop-back entire messages for self-test purposes. The received data can be read from the data table associated with the command.

4.2.20 ENCODER COMMAND TRANSMIT REQUEST Address: 25 W RT

Writing (any value) to this address causes the contents of the ENCODER DATA REGISTER to be sent as a command word. This instruction is useful for sending commands to the decoder while in loop-back mode. The command can then be read from the LAST COMMAND register.

4.2.21 EXTERNAL TERMINAL ADDRESS REGISTER Address: 30 R RT

This register contains information about the hardwire terminal address.

15	14	13	12	11	10	9	8
X	X	X	X	X	X	X	X
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INVALP	DISCONN	TADRP	TADR4	TADR3	TADR2	TADR1	TADR0

X = NOT USED

The terminal address may be hardwired using I/O DAT(5:0). External pull-down resistors of 4.7K are used to set a low, 64K internal pull-ups set a high. I/O DAT5 is wired for odd parity in the address. The hardwire terminal address and its parity can be obtained by reading I/O address 30. This address is unique since a read operation activates both the I/O bus command strobe and the I/O bus read signal (i.e., CMDS=1 and *I/O RD=0). As a result, a buffer containing the terminal address can be selected without decoding address lines. If an external buffer is not desired, pull-up/down resistors on the I/O data bus can be used instead (see BASIC STATUS register for details). The protocol chip also calculates the terminal address's parity and compares it to the value obtained from the I/O bus.

INVALP
INVALP = 1 specifies that the terminal address which was read automatically by the protocol chip following reset (from I/O address 30) had invalid parity.

DISCONN
DISCONN = 0 specifies that the store is disconnected because a terminal address of 31 was detected on the I/O bus for at least 800 nanoseconds.
DISCONN = 1 specifies that the store is connected.

This bit indicates the "disconnected store" condition defined by MIL-STD-1760A, provided that the store contains the pull-down resistors used for defining the terminal address (see BASIC STATUS register for details). After the store is disconnected, the standby state of all I/O lines will be high and will therefore define an illegal terminal address of 31.

TADRP
TADRP equals the value of the terminal address parity read from I/O address 30.

TADR
TADR equals the value of the terminal address read from I/O address 30.

4.2.22 COMMAND OUTPUT PINS — Address: 30 — W — RT

Writing a word to the COMMAND OUTPUT PINS (address 30 in the I/O space) can be used to simulate the option which outputs 5 bits onto the I/O bus following valid command reception (see CMDO bit in the CONTROL register for details). This address is unique since a write operation activates both the I/O bus COMMAND STROBE and the I/O bus write signal (i.e., CMDS=1 and *I/O WR=0). As a result, the bits can be latched without decoding address lines.

4.2.23 I/O TAG WORD REGISTER — Address: 30 — R/W — RT

When a data table is mapped to address 32 in the I/O space, its tag word is contained in this register. This tag word can be used, for example, to specify an output pulse whenever the data table is accessed. All other I/O space data tables are without internal tag words and have no pulses associated with them.

4.2.24 CONFIGURATION REGISTER 1 — Address: 9 — R/W — BC/MT/RT

This register is used to configure the functionality of the part.

15	14	13	12	11	10	9	8
MT_TYPE	GLOBAL BUS_SEL1	GLOBAL BUS_SEL0	FRAME_BLK	START BC_MT	3818 Status	FUNCTION SEL1	FUNCTION SEL2

7	6	5	4	3	2	1	0
0	0	INH_DBCA	ENA GLOBAL_DBS	ENA LOCAL_DBS	INH SOFT_ADR	BUSY_CONV	SEP_BCST_TBL

Note: Reserved Bits 7-6 must be set to "0".

MT_TYPE **Bits: 15** **MT**

0 = Word Monitor.
1 = Message Monitor .

GLOBAL_BUS_SEL **Bits: 14, 13** **BC**

These bits determine the Bus select options.

BUS OPTION	COMMENTS	14	13
DEFAULT	USE BC CONTROL WORD BUS	0	0
FORCE "A" BUS	ALL MESSAGES ON BUS "A"	0	1
FORCE "B" BUS	ALL MESSAGES ON BUS "B"	1	0
FORCE ALT BUS	IF "A" USE "B"; IF "B" USE "A"	1	1

FRAME/BLOCK **Bits: 12** **BC/MT**

0 = Frame "A" or Block "A".
1 = Frame "B" or Block "B".

START_BC_MT **Bits: 11** **BC/MT**

1 = Start BC or MT.

3818_STATUS **Bits: 10** **RT**

0 = Status response and protocol operation as defined in Mil-Std-1553B.
1 = Status response and protocol operation as defined in MDC A3818 and Mil-Std-1553A.

FUNCTION_SEL **Bits: 9, 8** **BC/MT/RT**

OPERATIONAL MODE	9	8
REMOTE TERMINAL	0	0
BUS CONTROLLER	0	1
MONITOR	1	0
MONITOR & REMOTE TERMINAL	1	1

INH_DBCA **Bits: 5** **RT**

0 = DBCA Bit in Status Word is set upon receipt of a valid DBCA Mode Code.
1 = Prevents DBCA Bit in Status Word from being set upon receipt of a valid DBCA Mode Code.

ENA_GLOBAL_DYNAMIC_BUS_SELECTION **Bits: 4** **BC**

0 = Message bus unchanged after successful Glocal Retry.
1 = Automatically switch message to alternate bus after successful retry on alternate bus of Global Retry option.

ENA_LOCAL_DYNAMIC_BUS_SELECTION **Bits: 3** **BC**

0 = Message bus unchanged after successful Local Retry.
1 = Automatically switch message to alternate bus after successful retry on alternate bus of Local Retry

option.

INH_SOFT_ADR **Bits: 2** **RT**

0 = Bits (15:11) of Basic Status Register set the RT Address when a Write Operation to that register is performed. The Hard Wired Address sets the RT Address at RESET.
1 = Prevents software change of RT Address when writing to the Basic Status Register. Bits (15:11) of Basic Status Register are "Don't Care". Only the Hard Wired Address sets the RT Address at RESET.

BUSY_CONV **Bits: 1** **RT**

0 = BUSY Bit is compliant with Mil-Std-1553B.
1 = Converts BUSY Bit to Non-1553B operation. BUSY Bit becomes a standard bit with no special functionality. BUSY Bit is not set during software reset or MODE CODE_08 RESET.

SEP_BCST_TABLES **Bits: 0** **RT**

0 = Broadcast messages use the same pointers as receive message:. therefore, receive and broadcast messages are stored in the same data tables. The BCST bit in the tag word is used to differentiate between the two message types.
1 = An additional 30 pointers are activated which puts receive and broadcast messages in separate data tables.

4.2.25 FRAME "A" POINTER / BLOCK "A" START — Address: 13 — R/W — BC/MT

This register contains the 16 bit FRAME "A" POINTER. This is the address of the active message list to be used by the BC or the MESSAGE MONITOR for FRAME "A".

In the WORD MONITOR, this register contains the 16 bit start address of BLOCK "A".

4.2.26 FRAME "A" LENGTH / BLOCK "A" END — Address: 14 — R/W — BC/MT

In the BC and MESSAGE MONITOR modes, this register specifies the number of messages in FRAME "A" message list and several END-OF-FRAME options.

In the WORD MONITOR, this register contains the 16 bit end address of BLOCK "A".

BUS CONTROLLER

15	14	13	12	11	10	9	8
RSVD	EOF_A_INT	STAT_SET STOP_A	FRAME_A ERR_STOP	FRAME_A END_OPT1	FRAME_A END_OPT0	FRAME_A LEN9	FRAME_A LEN8
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FRAME_A LEN7	FRAME_A LEN6	FRAME_A LEN5	FRAME_A LEN4	FRAME_A LEN3	FRAME_A LEN2	FRAME_A LEN1	FRAME_A LEN0

MESSAGE MONITOR

15	14	13	12	11	10	9	8
RSVD	EOF_A_INT	RSVD	RSVD	FRAME_A END_OPT1	FRAME_A END_OPT0	FRAME_A LEN9	FRAME_A LEN8
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

FRAME_A LEN7	FRAME_A LEN6	FRAME_A LEN5	FRAME_A LEN4	FRAME_A LEN3	FRAME_A LEN2	FRAME_A LEN1	FRAME_A LEN0

EOF_A_INT **Bits: 14** **BC/MT**

1 = The BC or the Message Monitor will interrupt when End of FAME "A" is reached.
0 = End of Frame **WILL NOT** cause an interrupt.

STATSET_STOP_A **Bits: 13** **BC**

1 = If any BC message in the frame causes a status bit set condition, then BC will stop at the end of the current frame and go off line.

FRAME_A_ERR_STOP **Bits: 12** **BC**

1 = If any BC message in the frame causes an error condition, then BC will stop at the end of the current frame and go off line.

FRAME_A_END_OPT **Bits: 11, 10** **BC/MT**

These two bits determine a course of action at the end of FRAME "A".

FRAME_A_END_OPTION	11	10
STOP_AT_END_OF_FRAME_A	0	0
REPEAT_FRAME_A	0	1
GOTO_FRAME_B	1	0
STOP_AT_END_OF_FRAME_A	1	1

FRAME_A_LENGTH **Bits: 9:0** **BC/MT**

These ten bits determine the number of messages that the frame will contain, up to a maximum of 1024.

4.2.27 **FRAME "B" POINTER** **Address: 16** **R/W** **BC/MT**
BLOCK "B" START

This register contains the 16 bit FRAME "B" POINTER. This is the address of the active message list to be used by the BC or the MESSAGE MONITOR for FRAME "B".

In the WORD MONITOR, this register contains the 16 bit start address of BLOCK "B".

4.2.28 **FRAME "B" LENGTH** **Address: 17** **R/W** **BC/MT**
BLOCK "B" END

In the BC and MESSAGE MONITOR modes, this regiater specifies the number of messages in FRAME "B" message list and several END-OF-FRAME options.

In the WORD MONITOR, this register contains the 16 bit end address of BLOCK "B".

15	14	13	12	11	10	9	8
RSVD	EOF_B_INT	STAT_SET STOP_B	FRAME_B ERR_STOP	FRAME_B END_OPT1	FRAME_B END_OPT0	FRAME_B LEN9	FRAME_B LEN8
7	6	5	4	3	2	1	0

FRAME_B LEN7	FRAME_B LEN6	FRAME_B LEN5	FRAME_B LEN4	FRAME_B LEN3	FRAME_B LEN2	FRAME_B LEN1	FRAME_B LEN0

MESSAGE MONITOR

15	14	13	12	11	10	9	8
RSVD	EOF_A_INT	RSVD	RSVD	FRAME_B END_OPT1	FRAME_B END_OPT0	FRAME_B LEN9	FRAME_B LEN8
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
FRAME_B LEN7	FRAME_B LEN6	FRAME_B LEN5	FRAME_B LEN4	FRAME_B LEN3	FRAME_B LEN2	FRAME_B LEN1	FRAME_B LEN0

EOF_B_INT **Bits: 14** **BC/MT**

1 = The BC or the Message Monitor will interrupt when End of FAME "B" is reached.
0 = End of Frame **WILL NOT** cause an interrupt.

STATSET_STOP_B **Bits: 13** **BC**

1 = If any BC message in the frame causes a status bit set condition, then BC will stop at the end of the current frame and go off line.

FRAME_B_ERR_STOP **Bits: 12** **BC**

1 = If any BC message in the frame causes an error condition, then BC will stop at the end of the current frame and go off line.

FRAME_B_END_OPT **Bits: 11, 10** **BC/MT**

These two bits determine a course of action at the end of FRAME "B".

FRAME_B_END_OPTION	11	10
STOP_AT_END_OF_FRAME_B	0	0
REPEAT_FRAME_B	0	1
GOTO_FRAME_A	1	0
STOP_AT_END_OF_FRAME_B	1	1

FRAME_B_LENGTH **Bits: 9:0** **BC/MT**

These ten bits determine the number of messages that the frame will contain, up to a maximum of 1024.

4.2.29 **BC_FRAME_GAP** **Address: 20** **R/W** **BC/MT**

WORD_MONITOR_EOF_OPTIONS

In the BC mode, this 16 bit register specifies the END_OF_FRAME_DELAY before starting the next frame. The delay resolution is 64 us.

In the WORD MONITOR, this register specifies the END-OF-FRAME options.

WORD MONITOR

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**

EOB_B INT	RSVD	BLOCK_B END_OPT1	BLOCK_B END_OPT0	EOB_A INT	RSVD	BLOCK_A END_OPT1	BLOCK_A END_OPT0

Note: Bits 15-8 are reserved and should be set to "0".

EOB_B_INT **Bits: 7** **MT**

1 = The Word Monitor will cause an interrupt when End of Block "B" is reached.
0 = End of Block **WILL NOT** cause an interrupt.

BLOCK_B_END_OPT **Bits: 5, 4** **MT**

These two bits determine a course of action at the end of BLOCK "B".

BLOCK_B_END_OPTION	5	4
STOP_AT_END_OF_BLOCK_B	0	0
REPEAT_BLOCK_B	0	1
GOTO_BLOCK_A	1	0
STOP_AT_END_OF_BLOCK_B	1	1

EOB_A_INT **Bits: 3** **MT**

1 = The Word Monitor will cause an interrupt when End of Block "A" is reached.
0 = End of Block **WILL NOT** cause an interrupt.

BLOCK_A_END_OPT **Bits: 1, 0** **MT**

These two bits determine a course of action at the end of BLOCK "A".

BLOCK_A_END_OPTION	1	0
STOP_AT_END_OF_BLOCK_A	0	0
REPEAT_BLOCK_A	0	1
GOTO_BLOCK_B	1	0
STOP_AT_END_OF_BLOCK_A	1	1

4.2.30 CONFIGURATION REGISTER 3 **Address: 21** **R/W** **BC/MT**

This register is used to set global parameters for the BC and the MT.

15	14	13	12	11	10	9	8
RSVD	WD_MT NO_TTAGDAT	WD_MT NO_TAG	WD_MT NO_TTAG	MSG_MT NO_TAG	MSG_MT NO_TTAG	GLOBAL RETRY1	GLOBAL RETRY0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
STAT_SET RETRY	ADR_LAT_INH	BCST_MSK BCST_XOR	BUS JAM_4	BUS JAM_3	BUS JAM_2	BUS JAM_1	BUS JAM_0

WD_MT_NO_TTAGDAT **Bits: 14** **MT**

0 = A 32 bit time tag is stored with data words and command/status words.
1 = No time tag on data words. Only command/status words are time tagged.

WD_MT_NO_TAG **Bits: 13** **MT**

0 = Tag word is stored with data and command/status words.
1 = No tag word.

WD_MT_NO_TTAG **Bits: 12** **MT**

0 = Word Monitor time tag is enabled. Bit 14 determines the time tag format.
1 = Word Monitor time tag is disabled.

MSG_MT_NO_TAG **Bits: 11** **MT**

0 = Tag word is stored with command/status words.
1 = No tag word.

MSG_MT_NO_TTAG **Bits: 10** **MT**

0 = Message Monitor time tag is enabled. Command/status words are time tagged.
1 = Message Monitor time tag is disabled.

GLOBAL_RETRY **Bits: 9, 8** **BC**

These bits define a global default retry scenario. If the BC control word defines no retry as the option for a message, then the global retry is enabled. If the global retry is defined as no retry, then their will not be a retry for the message.

GLOBAL_RETRY	9	8
NO_RETRY	0	0
RETRY_ACTIVE_BUS	0	1
RETRY_ALT_BUS	1	0
RETRY_ALT_BUS THEN_ACTIVE_BUS	1	1

STATUS_SET_RETRY **Bits: 7** **BC**

This bit determines if a retry will be executed when a status word invokes a status set condition.
0 = No retry on status set.
1 = Retry if a status bit is set.

ADR_LAT_INH **Bits: 6** **RT**

This bit determines whether or not the CPU address will be automatically latched by the HCS_L.
0 = CPU address is automatically latched within 200ns after the falling edge of HCS_L.
1 = CPU address is manually stored in a transparent when ADR_LAT_L input signal is a "1".

BCST_MSK/BCST_XOR **Bits: 5** **RT**

This bit determines how the BCST bit in the status word will be treated.

0 = If the BCST bit in the status word **DOES NOT** equal bit 4 of ths BC CONTROL WORD, then the STAT_SET bit in the BC CONTROL WORD will be set.

1 = If bit 4 of the BC CONTROL WORD is a "0", then the BCST bit in the status word is **DON'T CARE.** If bit 4 of the BC CONTROL WORD IS a "1" and the BCST bit in the status word is a "1", then the STAT_SET bit in the BC CONTROL WORD will be set.

BUS_JAM **Bits: 4:0** **BC**

These bits determine the number of excess words that will be accepted from an RT without declaring that the bus has been jammed by an RT that is transmitting continuously. The range is from 0 to 31 words. The msb is bit 4. When a **BUS_JAM** is detected, the BC issues a non-maskable interrupt by setting the PLSCMD_BSJM_H output pin to a "1" and Halts.

The CPU can cause the BC to continue by writing to one of the bits in CONFIGURATION REGISTER 2 after taking corrective action (ie: Globally switch all messages to good bus using Config Reg 1).

4.2.31 MT ADDRESS FILTER (RT15-RT0) Address: 22 R/W MT

This register determines which RT addresses, from 0 to 15 will be monitored in the MESSAGE MONITOR mode.

0 = Accept RT address, store data.
1 = Ignore RT address, **NO** data stored.

15	14	13	12	11	10	9	8
RTMSK_15	RTMSK_14	RTMSK_13	RTMSK_12	RTMSK_11	RTMSK_10	RTMSK_09	RTMSK_08
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RTMSK_07	RTMSK_06	RTMSK_05	RTMSK_04	RTMSK_03	RTMSK_02	RTMSK_01	RTMSK_00

4.2.32 MT ADDRESS FILTER (RT31-RT16) Address: 26 R/W MT

This register determines which RT addresses, from 16 to 31 will be monitored in the MESSAGE MONITOR mode.

0 = Accept RT address, store data.
1 = Ignore RT address, **NO** data stored.

15	14	13	12	11	10	9	8
RTMSK_31	RTMSK_30	RTMSK_29	RTMSK_28	RTMSK_27	RTMSK_26	RTMSK_25	RTMSK_24
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RTMSK_23	RTMSK_22	RTMSK_21	RTMSK_20	RTMSK_19	RTMSK_18	RTMSK_17	RTMSK_16

4.2.33 BLOCK "A" LAST ADDRESS Address: 27 R MT

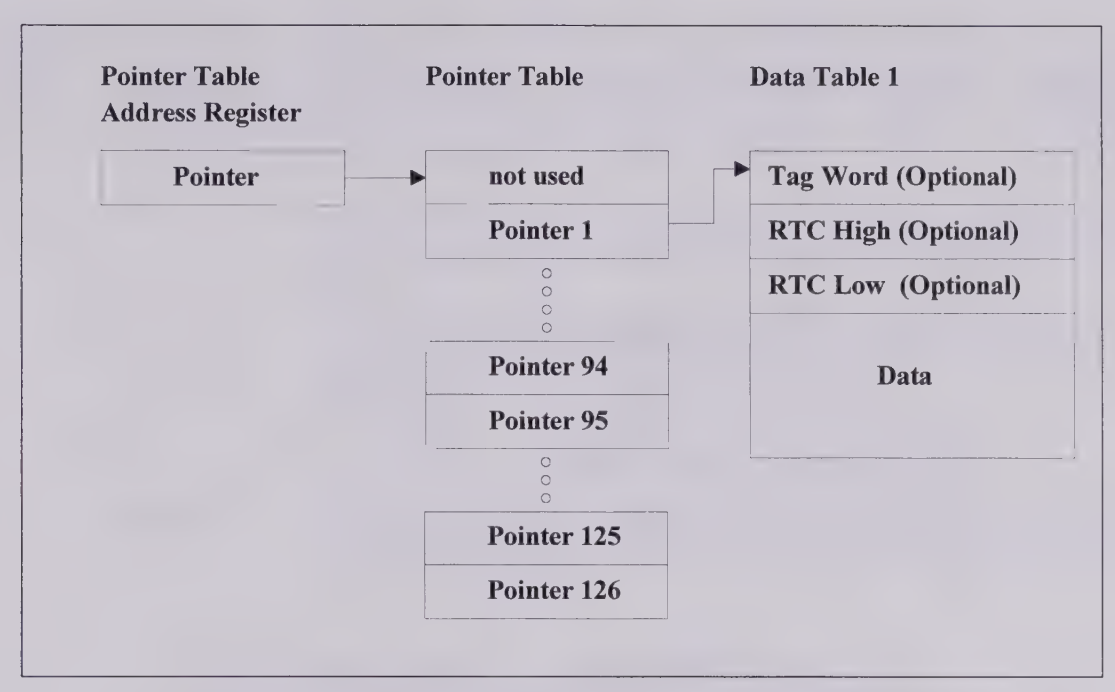
This register contains the address of the last word in BLOCK "A" for the WORD MONITOR. The last address is calculated by the protocol chip. It is not necessarily equal to the BLOCK "A" end address in register 14. This is because any one of up to four words associated with the last in-coming word in the block could be stored in register 14. In order to keep all the words together, they are stored contiguously and the last address in BLOCK "A" is stored in this register; therefore, four addresses must always be reserved after the address in register 14 to accommodate this situation.

4.2.34 BLOCK "B" LAST ADDRESS Address: 28 R MT

This register contains the address of the last word in BLOCK "B" for the WORD MONITOR. The last address is calculated by the protocol chip. It is not necessarily equal to the BLOCK "B" end address in register 17. This is because any one of up to four words associated with the last in-coming word in the block could be stored in register 17. In order to keep all the words together, they are stored contiguously and the last address in BLOCK "B" is stored in this register; therefore, four addresses must always be reserved after the address in register 17 to accommodate this situation.

4.3.0 RT DATA TABLES

The data words associated with transmit/receive/broadcast messages and mode commands are stored in data tables. The data table addresses are stored in a POINTER TABLE located in the RAM. The data tables themselves can be individually allocated to either the RAM or the I/O space. Data tables mapped to the I/O space can be used for discrete I/O without requiring host intervention. The mapping scheme is illustrated in the following diagram:



The address, T/R, subaddress, and word count fields in the command are used to index the pointer table as defined below:

Index	T/R	Subaddress	Mode Code	Command Type
0		not used		
1-30(31)	0	1-30(31)		Receive - Broadcast
31-32		not used		
33-62	1	1-30(31)		Transmit
63		Note 2		
64-95	X	0,31	0-31	Mode Codes
96		not used		
97-126	0	1-30(31)		Broadcast

Note 1: Separate Broadcast Pointers are activated when BIT "0" of CONFIGURATION REGISTER 1 is a "1" (See this register for details).
Note 2: When 3818A/1553A protocol option is enabled, subaddress 31 is an extend subaddress, **Not a Mode Code Flag.**

4.3.1 MESSAGE ILLEGALITY

Commands are illegalized by setting the address field of the corresponding data table pointer to 0. When the protocol chip receives an illegal command, it responds with ME=1 in the status; in addition, data transmission and storage are suppressed. All undefined mode commands as well as "Dynamic Bus Control" are ignored.

4.3.2 DATA TABLE TAG WORD

The data table's first word can be defined to be either a data word or a TAG WORD (see the NTAG field in the CONTROL register) which defines the table's status and associated options. The TAG WORD has the following format:

15	14	13	12	11	10	9	8
UPD	SSFENA	BCST	X	PULSE_3	PULSE_2	PULSE_1	PULSE_0
7	6	5	4	3	2	1	0
LOCK	INV	OVW	WCNT_4	WCNT_3	WCNT_2	WCNT_1	WCNT_0

UPD 1 Indicates that the table was updated with data by the host or a 1553 message. The host should set this bit after writing to the table and reset the bit after reading the table.

SSFENA 1 Enables setting the subsystem flag in the status word whenever the RT transmits stale data or overwrites received data (i.e., whenever data is transmitted from a table with UPD=0, or is stored into a table with UPD=1).

BCST 1 Indicates that the table contains data from a valid broadcast message.

0 Indicates that the table contains data from a non-broadcast message.

PULSE(3:0) This field defines which pin should be pulsed at the end of a valid message which accesses the data table (see CMDO in the CONTROL register for details). The field is defined as follows:

PULSE FIELD VALUE	PULSED OUTPUT PIN
0	No Pulse
1-8	I/O DATA(0),...,(7)
14	PLSCMD

LOCK 1 Indicates that the protocol chip is currently using the table for a message, either writing receive data or reading transmit data.

INV 1 Indicates that the table contains invalid data.

OVW 1 Indicates that data received from the 1553 bus caused the data to be overwritten before its previous contents were read by the host or that the host did not update the data since the last transmission (i.e., whenever data is transmitted from a table with UPD=0, or is stored into a table with UPD=1). This bit is similar to the subsystem flag returned to the Bus Controller when SSFENA=1.

WCNT(4:0) This field contains the word count/mode code in the command which referenced the data table.

4.3.3 DATA TABLE POINTER

The DATA TABLE POINTER has the following format:

15	14	13	12	11	10	9	8
INTREQ	RTCENA_1	ADDR_13	ADDR_12	ADDR_11	ADDR_10	ADDR_9	ADDR_8
7	6	5	4	3	2	1	0
ADDR_7	ADDR_6	ADDR_5	ADDR_4	ADDR_3	ADDR_2	ADDR_1	RTCENA_0

INTREQ 1 Specifies that an interrupt shall be issued after the completion of a message which accesses the data table.

ADDR(13:1) Defines the location of the data table in the lower 8K word address space. Since data tables always begin on word boundaries, the register's LSB (which specifies byte boundaries) is ignored. If the address field is set to 0, the command associated with the pointer is illegalized.

RTCENA(1:0) Real Time Clock Time Tag Message Oprions. The Time_Tag_Transmit option will cause the first two transmitted words of the associated Transmit Command to contain the time tag, MSW first.

OPERATIONAL MODE	COMMENTS	14	0
NO_TIME_TAG	NO TIME TAG ON MESSAGE	0	0
NO_TIME_TAG	NO TIME TAG ON MESSAGE	0	1
TIME_TAG_DON'T_TRANSMIT	DO NOT TRANSMIT TIME TAG AS DATA	1	0
TIME_TAG_TRANSMIT	TRANSMIT TIME TAG AS DATA	1	1

4.3.4 RT DATA TABLE BUFFERING SCHEME

Since the host and the NHI_ ET can access data tables asynchronously, data integrity must be ensured by a suitable buffering scheme. The method employed by the ET assumes that there are two pointer tables; one specifies data tables accessed by the RT and the other tables accessed by the host. The host's pointer table can reside anywhere in its memory space since it is never accessed by the ET. Data buffers are switched by the host exchanging pointers as explained below.

4.3.4.1 RT RAM ACCESS

When the ET wants to read or write to a data table, it fetches the corresponding data table pointer from its pointer table. It then sets the LOCK bit in the data table's TAG WORD to 1 and proceeds with the update. At the completion of the update, the ET sets the LOCK bit to 0 and also sets the UPD bit in the TAG WORD to 1 if it wrote to the data table or 0 if it read the data table. If the condition of the UPD bit at the start of the ET access indicates that the host has not read from or written to the data table since the last ET access to that table, the ET sets the OVW bit in the TAG WORD to 1 to tell the host stale data has been transmitted by the ET or data has been overwritten by the ET.

Since the ET may fetch a data table pointer while the host is in the process of exchanging the corresponding pointers, there is a possibility that the ET's pointer will point to the table used by the host. In order to avoid this potential conflict, the host should check the LOCK bit in its data table tag word AFTER exchanging the pointers but BEFORE reading the data. If LOCK=1, the host should wait until the protocol chip LOCK=0.

NOTE: The LOCK bit is ALWAYS set in the TAG WORD of the data table accessed by the ET, irrespective of when the pointers are exchanged by the host. This is guaranteed because the ET reads the data table's pointer and sets the LOCK bit in the TAG WORD using a read - read - modify - write sequence which cannot be interrupted by the host (i.e., read POINTER - read TAG WORD - modify LOCK bit - write back TAG WORD with LOCK bit modified).

4.3.4.2 HOST RAM ACCESS

When the host wants to access a RECEIVE data table, it first exchanges the pointer in its pointer table with the corresponding pointer in the ET's table. Then, the host reads the LOCK bit in the TAG WORD. If the LOCK bit is 0, the host proceeds with its access. If, however, the LOCK bit is 1, this informs the host that the ET is accessing that data table. The host should then delay its access until the LOCK bit has been set to 0 by the ET. When the host finishes accessing the RECEIVE data table, it should clear the UPD bit in the data table's TAG WORD to 0. This will tell the ET the host has taken the data.

When the host wants to access a TRANSMIT data table, it first reads the LOCK bit in the TAG WORD of the table belonging to the host. If the LOCK bit is 0, the host proceeds with its access. If, however, the LOCK bit is 1, this informs the host that the ET is still accessing that data table. The host should then delay its access until the LOCK bit has been set to 0 by the ET. When the host finishes updating its TRANSMIT data table, it should set the UPD bit in the data table's TAG WORD to 1 and then exchange corresponding

pointers. This will ensure that updated data for transmission is made available to the ET as soon as possible and inform the ET that it will be transmitting fresh data.

Since the host can change its table of pointers at any time, the above mapping scheme can be used to achieve any desired depth of buffering by simply employing a "round-robin" of pointers.

4.3.4.3 READ-MODIFY-WRITE

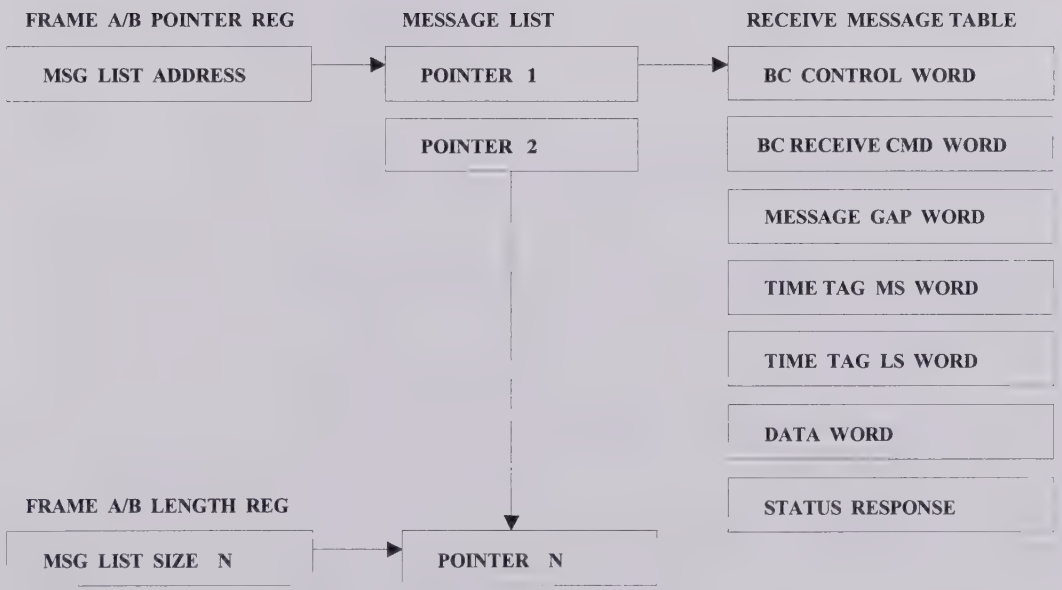
The host Read-Modify-Write cycle is used to support CPUs similar to the Motorola 680X0 where certain instructions (eg:, test and set) require two contiguous accesses to memory. Such accesses are unique in that the address remains active for both cycles.

4.4.0 BC MESSAGE LISTS AND DATA TABLES

The BC is organized and controlled by message lists. Each message list contains the addresses of data tables associated with the list. A message list can contain up to a maximum of 1024 16 bit addresses. The number of message lists and data tables is limited only by the size of the ram. The message list mapping scheme is illustrated in FIGURE 4.4.1. FRAME A/B POINTER and FRAME A/B LENGTH registers have been discussed in a previous section. See details.

The CPU loads each message list with number of message table pointers determined by a given scenario requirement. The list is activated by placing its address in the FRAME A or FRAME B POINTER register and the number of pointers in the list in the corresponding FRAME LENGTH register.

BUS CONTROLLER MEMORY ORGANIZATION EXAMPLE



4.4.1 BC CONTROL WORD

The BC CONTROL WORD contains information which is specific to the message in its data table. The word has certain bits which are controlled by the CPU and others are controlled by the ET. This dual functionality provides a more a friendly and uncomplicated user inter face. Bits(9:0) are defined by the CPU and provide message setup detail, while Bits(15:10) are controlled by the ET and report operation information.

15	14	13	12	11	10	9	8
EOM	RETRY	STAT_SET	ERROR	NO_RESP	SOM	LCL_RTY1	LCL_RTY0
7	6	5	4	3	2	1	0
BUS	TF_RSVD_INST	SRQ	BCST	BUSY	SSF	MSG_ERR	RT_RT

EOM 1 **Set by the ET.** Message has been transmitted and completed.

RETRY 1 **Set by the ET.** A Retry has been attempted for this message. See LOCAL and GLOBAL retry setups for the scenario.

STAT_SET 1 **Set by the ET.** The Status word returned by the RT had one or more bits set.

ERROR 1 **Set by the ET.** The message returned by the RT contained an error.

NO_RESP 1 **Set by the ET.** The RT DID NOT respond with a Status word as expected.

SOM 1 **Set by the ET.** The message is currently active. The ET could be transmitting, waiting for a response or receiving.

LOCAL_RETRY **Set by the CPU.** Bits(9:8) define a local specific retry scenario. If the BC control word defines no retry as the option for the message, then the global retry is enabled. If the global retry is defined as no retry, then their will not be a retry for the message.

LOCAL_RETRY	9	8
NO_RETRY	0	0
RETRY_ACTIVE_BUS	0	1
RETRY_ALTERNATE_BUS	1	0
RETRY_ALTERNATE_BUS THEN_ACTIVE_BUS	1	1

BUS 0 **Set by the CPU.** Message will use BUS A.

1 Message will use BUS B. This bit defines the bus that the message will use. This bus setting, however, can be overridden by the settings in CONFIGURATION 1. See this register for specific details.

TF_RSVD_INST 0 **Set by the CPU.** The value of the Terminal Flag bit, the Reserved bits, and the Instrumentation bit are treated as "Don't Care", and will NOT cause the STAT_SET bit to be set no matter what their value in the returned Status word.

1 The STAT_SET bit will be set if the Terminal Flag bit, or one of the Reserved bits or the instrumentation bit is set in the returned Status word.

SRQ 0 **Set by the CPU.** The value of the Service Request bit is treated as "Don't Care", and will NOT cause the STAT_SET bit to be set no matter what its value in the returned Status word.

1 The STAT_SET bit will be set if the Service Request bit is set in the returned Status word.

BCST **Set by the CPU.** The operation of this bit is determined by bit 5 of CONFIGURATION REGISTER 3. This bit will either be used as a mask or an xor flag for the Broadcast Received bit in the returned status word.

CNFG3_05 = 0 (bit 4 is an xor flag):

If the Broadcast Received bit in the returned status word **DOES NOT** equal bit 4 of the BC CONTROL WORD, then the STAT_SET bit in the BC CONTROL WORD will be set.

CNFG3_05 =1 (bit 4 is a mask):

0 The value of the Broadcast Received bit is treated as "Don't Care", and will NOT cause the STAT_SET bit to be set no matter what its value in the returned Status word.

1 The STAT_SET bit will be set if the Broadcast Received bit is set in the returned Status word.

BUSY

0 **Set by the CPU.** The value of the Busy bit is treated as "Don't Care", and will NOT cause the STAT_SET bit to be set no matter what its value in the returned Status word.

1 STAT_SET bit will be set if the Busy bit is set in the returned Status word.

MSG_ERR

0 **Set by the CPU.** The value of the Message Error bit is treated as "Don't Care", and will NOT cause the STAT_SET bit to be set no matter what its value in the returned Status word.

1 The STAT_SET bit will be set if the Message Error bit is set in the returned Status word.

SSF

0 **Set by the CPU.**
The value of the Subsystem Flag bit is treated as "Don't Care", and will NOT cause the STAT_SET bit to be set no matter what its value in the returned Status word.

1 The STAT_SET bit will be set if the Subsystem Flag bit is set in the returned Status word.

RT_RT

0 **Set by the CPU.** Message is **NOT** an RT to RT command.

1 Message **IS** an RT to RT command.

4.4.2 BC COMMAND WORD

This is the 16 bit 1553 Command word that defines the message type.

4.4.3 BC MESSAGE GAP WORD

The BC MESSAGE GAP WORD contains additional information which is specific to the message in its data table. The word sets the gap time delay to the start of the next message in the list, end of message stop conditions, the message interrupt and a NOP feature. The resolution of the Gap counter is 1us and the maximum gap is 4ms. NOP's can be used to extend the inter-message gap beyond the 4ms maximum which is allowed by the Gap field.

15	14	13	12	11	10	9	8
NOP	INT_EOM	STAT_STOP	ERROR_STOP	GAP_11	GAP_10	GAP_09	GAP_08
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
GAP_07	GAP_06	GAP_05	GAP_04	GAP_03	GAP_02	GAP_01	GAP_00

NOP

0 Send message as defined.

1 Do NOT send message. Start Gap Timer and wait till time out, then GoTo next message.

INT_EOM

0 **No** interrupt at End-of-Message.

1 **Interrupt** at End-of-Message.

STAT_STOP 1 Halt and go off-line if a Status Set is detected in any RT status word.

ERROR_STOP 1 Halt and go off-line if an Error is detected in any message.

GAP(11:0) This field sets the Gap Time delay. The resolution is 1us and the range of the delay is 0 to 4ms. The start of the next message in the list is delayed by this interval.

4.4.4 BC TIME TAG MS WORD

This word contains the upper 16 bits of the 32 bit Time Tag.

4.4.5 BC TIME TAG LS WORD

This word contains the lower 16 bits of the 32 bit Time Tag.

4.4.6 BC DATA WORD

This space contains from 1 to 32 data words which are associated with the message.

4.4.7 BC STATUS RESPONSE

This space contains the Status response from the RT

4.4.8 BC MESSAGE TABLE FORMATS

RECEIVE COMMAND
BC Control Word
Receive Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
Data Word(s)
RT Status Response

BCST RECEIVE COMMAND
BC Control Word
Receive Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
Data Word(s)

RT-RT COMMAND
BC Control Word
Receive Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
Transmit Command Word
Transmit RT Status Response
Data Word(s)
Receive RT Status Response

BCST RT-RT COMMAND
BC Control Word
Receive Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
Transmit Command Word
Transmit RT Status Response
Data Word(s)

TRANSMIT COMMAND
BC Control Word
Transmit Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
RT Status Response
Data Word(s)

TRANSMIT MODECODE Without DATA
BC Control Word
Transmit Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
RT Status Response

TRANSMIT MODECODE With DATA
BC Control Word
Transmit Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
RT Status Response
Data Word

RECEIVE MODECODE COMMAND
BC Control Word
Receive Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
Data Word
RT Status Response

BCST RECEIVE MODECODE COMMAND
BC Control Word
Receive Command Word
Message Gap Word
TimeTag MS Word
TimeTag LS Word
Data Word

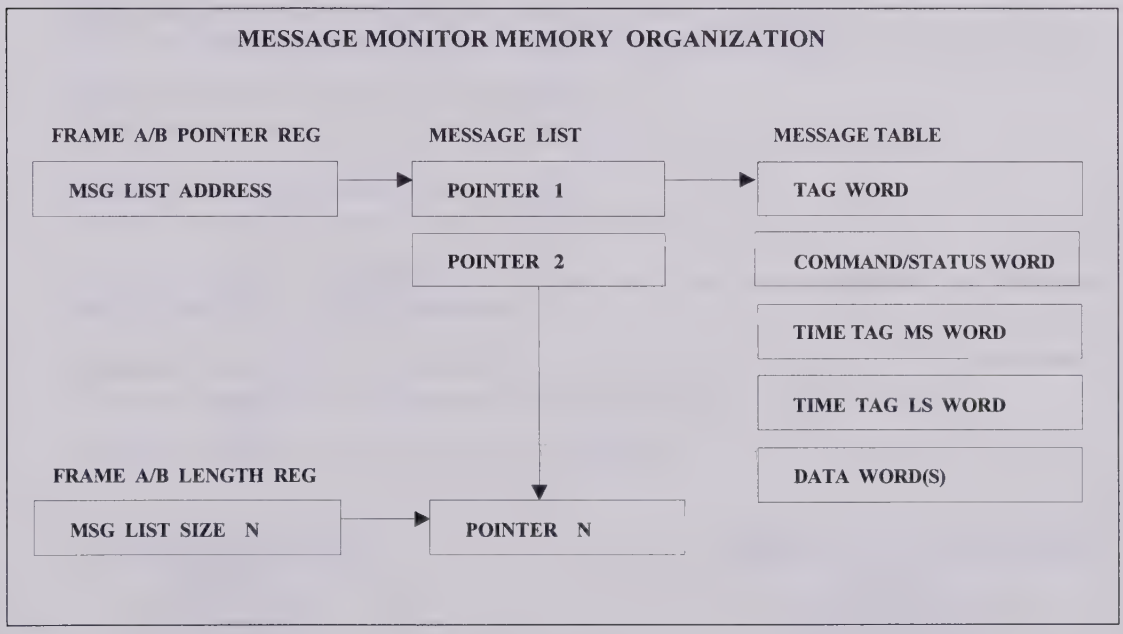
4.5.0 MESSAGE MONITOR MESSAGE LISTS AND DATA TABLES

The Message Monitor is organized and controlled by message lists, very similar to the BC mode. Each message list contains the addresses of data tables associated with the list. A message list can contain up to a maximum of 1024 16 bit addresses. The number of message lists and data tables is limited only by the size of the ram. The message list mapping scheme used by the monitor is illustrated in FIGURE 4.5.1. FRAME A/B POINTER and FRAME A/B LENGTH registers have been discussed in a previous section. See details.

The CPU loads the first pointer in each message list. The list is activated by placing its address in the FRAME A or FRAME B POINTER register and the list length in the corresponding FRAME LENGTH register. The ET will calculate all succeeding pointers in the list as it creates message tables . When the number of pointers is equal to the list length the frame terminates.

Messages can be filtered by RT address. This is accomplished with the two MONITOR ADDRESS FILTER REGISTERS. See them for details.

The MESSAGE MONITOR begins storing a message when it detects a command sync, providing the RT address has been enabled in the MONITOR ADDRESS FILTER REGISTERS, and stops storing the message when a gap is detected.



4.5.1 MESSAGE MONITOR TAG WORD

The MESSAGE MONITOR TAG WORD contains information which is specific to the message in its data table. The ET loads these bits as the message is processed.

The TAG WORD is optional and it can be suppressed from the message table. See the CONFIGURATION 3 for details.

15	14	13	12	11	10	9	8
EOM	0	WC_5	WC_4	WC_3	WC_2	WC_1	WC_0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUS	OVRLP	SOM	SYNC_ERR	DATA_ERR	CMD2_ERR	CMD1_ERR	RT_RT

Note: Bit 14 is reserved and always reads 0.

EOM	1	Complete message has been stored in the ram.
WC(5:0)		This six bit field represents the total number of words in the message table.
BUS	0	Message received on bus "A".
	1	Message received on bus "B".
OVRLP	1	A message was detected on the alternate bus before the message on the current bus was completed. The monitor aborts processing the current message, switches to the alternate bus, and begins processing the new message.
SOM	1	Message is currently active and being stored in the ram.
SYNC_ERR	1	A contiguous word was received with a command sync.
DATA_ERR	1	A data word contained an error (encoding, parity, bit count, etc).
CMD2_ERR	1	The second command word in an RT-RT command contained an error (encoding, parity, bit count, etc).
CMD1_ERR	1	The first command word in an RT-RT command contained an error (encoding, parity, bit count, etc).
RT-RT	1	The command is an RT-RT message.

4.5.2 MESSAGE MONITOR COMMAND - STATUS WORD

This is the command or status word that triggered the message monitor to start storing the message.

4.5.3 MESSAGE MONITOR TIME TAG MS WORD

This word contains the upper 16 bits of the 32 bit Time Tag.

4.5.4 MESSAGE MONITOR TIME TAG LS WORD

This word contains the lower 16 bits of the 32 bit Time Tag.

Note: The two TIME TAG WORDS are optional and they can be suppressed from the message table. See the CONFIGURATION 3 for details.

4.5.5 MESSAGE MONITOR DATA WORDS

This space contains from 1 to 32 data words which may be associated with the message.

4.5.6 MESSAGE MONITOR MESSAGE TABLE FORMATS

RECEIVE COMMAND
Tag Word
Command Word
TimeTag MS Word
TimeTag LS Word
Data Word(s)

RECEIVE STATUS RESPONSE
Tag Word
Status Response Word
TimeTag MS Word
TimeTag LS Word

TRANSMIT COMMAND
Tag Word
Command Word
TimeTag MS Word
TimeTag LS Word

TRANSMIT STATUS RESPONSE
Tag Word
Status Response Word
TimeTag MS Word
TimeTag LS Word
Data Word(s)

RT-RT COMMAND
Tag Word
Command Word 1
TimeTag MS Word

RT-RT STATUS 1 RESPONSE
Tag Word
Status Response Word
TimeTag MS Word

TimeTag LS Word
Command Word 2

TimeTag LS Word
Data Word(s)

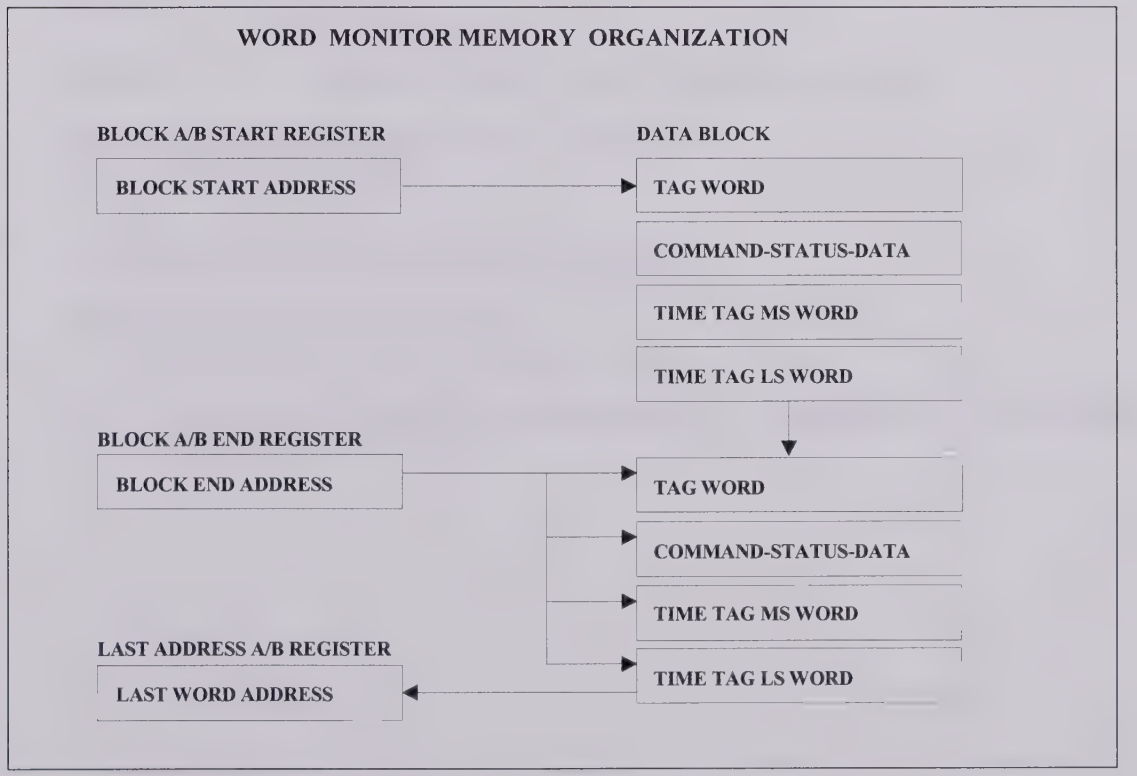
RT-RT STATUS 2 RESPONSE
Tag Word
Status Response Word
TimeTag MS Word
TimeTag LS Word

4.6.0 WORD MONITOR DATA TABLES

The Word Monitor is organized and controlled by two registers, the BLOCK A/B START and the BLOCK A/B END registers. The data table mapping scheme used by the monitor is illustrated in FIGURE 4.6.1.

In the figure, the Block Start register contains the address of the start of the data block, while the Block End register contains the end address of the data block; therefore, the amount of ram used by the data block is defined by these two registers. Notice, however, that the Block End register can contain the address of any one of the four words associated with the last word monitored in the block. This is a result of keeping the last four words in contiguous ram locations. The last address register, though, always contains the address of the last word in the data block. The address in this register is calculated by the ET and place in the Last Address register which is read only; therefore, when defining the ram space for a data block in the word monitor, always leave the next four locations after the block end address open. This will provide the reserve memory required to keep all the data in the block contiguous.

All the data in a data block is stored in consecutive addresses, starting with the user supplied block start address and ending with the monitor calculated last word address.



4.6.1 WORD MONITOR TAG WORD

The WORD MONITOR TAG WORD contains information which is specific to the current word taken from the bus and stored in the data table. The ET loads these bits as the word is processed.

The TAG WORD is optional and it can be suppressed from the message table. See the CONFIGURATION 3 for details.

15	14	13	12	11	10	9	8
GAP_7	GAP_6	GAP_5	GAP_4	GAP_3	GAP_2	GAP_1	GAP_0
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BUS	OVRLP	0	0	BCST	SYNC	ERROR	GAP_DET

GAP(7:0) This field contains the time interval in microseconds between its associated bus word and the preceding bus word. The resolution of the time interval is 0.5us. If the gap is greater than or equal to 127.5us, then this field will hold at 127.5us. this field is valid only if bit 4 is a "1".

BUS
0 Word was received on bus "A".
1 Word was received on bus "B".

OVRLP 1 A message was detected simultaneously on both busses . The Bus Monitor switches to the most current bus.

GAP_DET
0 This word was contiguous with the previous bus word. Ignore bits (15 - 8).
1 There was a gap between this word and the previous bus word. The gap time is recorded bits (15 - 8).

BCST
0 Broadcast address **NOT** detected.
1 Broadcast address **WAS** detected in bus word.

SYNC
0 Data sync.
1 Command sync.

ERROR 1 Bus word contained an error - encoding, parity, bit count, etc.

4.6.2 WORD MONITOR COMMAND - STATUS - DATA

This is the word read from the bus.

4.6.3 WORD MONITOR TIME TAG MS WORD

This word contains the upper 16 bits of the 32 bit Time Tag.

4.6.4 WORD MONITOR TIME TAG LS WORD

This word contains the lower 16 bits of the 32 bit Time Tag.

Note: The two TIME TAG WORDS are optional and they can be suppressed from the data table. See the CONFIGURATION 3 for details.

5.0.0 RT MODE CODE OPERATION

5.1.0 GENERAL

This section will define the operation of the NHI-ET when operating as an RT during reception of all the mode commands. The following terms are used in this section:

VALID COMMAND
A command meeting the criteria established by the 1553B standard in paragraph 4.4.1.1.

INVALID COMMAND
A command NOT meeting the criteria established by the 1553B standard in paragraph 4.4.1.1.

UNIMPLEMENTED COMMAND
A command not implemented by the NHI-ET.

The following general response characteristics apply to the NHI-ET when operating on the bus:

RECEIPT OF AN INVALID COMMAND
There is no response and the command is ignored.

RECEIPT OF AN UNIMPLEMENTED COMMAND
There is no response and the command is ignored.

The following abbreviations are used in this discussion:

SW = STATUS REGISTER
CDR = CONDITION REGISTER
TW = TAG WORD IN DATA TABLE
ME = MESSAGE ERROR BIT
BCR = BROADCAST BIT

Additional information about each mode code is available in the INTERRUPT VECTOR REGISTER and the AUXILIARY VECTOR REGISTER if it is set to be interrupt driven (see Data Table Pointer word, Interrupt Vector Register and Auxiliary Vector Register).

The following table describes the response and the action taken by the NHI-RT to all of the mode codes.

5.2.0 TABLE OF MODE CODE RESPONSES

5.2.1 DYNAMIC BUS CONTROL (00000; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

BROADCAST
UNIMPLEMENTED COMMAND

5.2.2 SYNCHRONIZE WITHOUT DATA (00001; T/R=1)

VALID COMMAND
Responds with status except if broadcast
Bits set: *MDCD to "0" in CDR
If broadcast- BCR, BCST in SW & TW to "1"

COMMAND+DATA WORD
No status response
Bits set: *MDCD to "0" in CDR. ME to "1" in SW
INV to "1" in TW

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.3 SYNCHRONIZE WITHOUT DATA (00001; T/R=1)

VALID COMMAND
Responds with status except if broadcast. Status NOT updated.
Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
Status not cleared. No status response.
Bits set: *MDCD to "0" in CDR. INV to "1" in TW.
ME to "1" in SW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.4 INITIATE SELF TEST (00011; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.5 TRANSMITTER SHUTDOWN (00100; T/R=1)

VALID COMMAND

Responds with status except if broadcast. Transmitter on alternate bus inhibited.
Alternate bus transmitter re-enabled by: Reset mode code, Override Transmitter Shutdown mode code, resetting RT, or power up. Bits set: *MDCD to "0" and alt bus (A) (B) XEN to "0" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.6 OVERRIDE TRANSMITTER SHUTDOWN (00101; T/R=1)

VALID COMMAND
Responds with status except if broadcast. Transmitter on alternate bus enabled.
Bits set: *MDCD to "0" and alt bus (A) (B) XEN to "1" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.7 INHIBIT TERMINAL FLAG (00110; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" and TFE to "0" in CDR. Terminal Flag inhibited in SW.

If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.8 OVERRIDE INHIBIT TERMINAL FLAG (00111; T/R=1)

VALID COMMAND

Responds with status except if broadcast.
Bits set: *MDCD to "0" and TFE to "1" in CDR. Terminal Flag enabled in SW.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.9 RESET REMOTE TERMINAL (01000; T/R=1)

VALID COMMAND
Responds with status except if broadcast. Both Transmitters enabled and Terminal Flag enabled. Pointer base address register set to 2048 dec. External terminal address loaded.
Bits set:
If broadcast- BCR, BCST in SW & TW set to "1".

COMMAND+DATA WORD
No status response.
Bits set:
INV to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.10 RESERVED MODE CODES (01001-01111; T/R=1)

VALID COMMAND
Responds with status except if broadcast.
Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME and BCR set to "1" in SW.
INV and BCST set to "1" in TW.

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.11 TRANSMIT VECTOR WORD (10000; T/R=1)

VALID COMMAND
Responds with status followed by vector word except if broadcast.
Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD
UNIMPLEMENTED COMMAND

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.12 SYNCHRONIZE WITH DATA WORD (10001; T/R=0)

VALID COMMAND
Responds with status except if broadcast. Data word stored into RAM. Data word will update lower 16 bits of real time clock depending on the configuration of the RTC CONTROL REGISTER.

Bits set: *MDCD to "0" in CDR.
If broadcast- BCR, BCST in SW & TW to "1".

COMMAND NO DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.

COMMAND + EXTRA DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV set to "1" in TW.

BROADCAST + EXTRA DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME and BCR to "1" in SW.
INV and BCST to "1" in TW.

T/R=1
UNIMPLEMENTED COMMAND

T/R=1 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.13 TRANSMIT LAST COMMAND (10010; T/R=1)

VALID COMMAND

Responds with status followed by LAST VALID COMMAND word except if broadcast.
Status and command registers NOT updated.

Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR.
INV to "1" in TW.
ME to "1" in SW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD
UNIMPLEMENTED COMMAND

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.14 TRANSMIT BIT WORD (10011; T/R=1)

VALID COMMAND
Responds with status followed by BIT word.
Bits set: *MDCD to "0" in CDR.

COMMAND+DATA WORD
No status response.
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD
UNIMPLEMENTED COMMAND

T/R=0
UNIMPLEMENTED COMMAND

T/R=0 AND BROADCAST
UNIMPLEMENTED COMMAND

5.2.15 SELECTED TRANSMITTER SHUTDOWN (10100; T/R=0)

VALID COMMAND
Responds with status except if broadcast.
Bits set:
If broadcast- BCR, BCST to "1" in TW & SW.

COMMAND + EXTRA DATA WORD
No response
Bits set:

INV to "1" in TW.

COMMAND WITHOUT DATA WORD
No response
Bits set:

BROADCAST WITH EXTRA DATA WORD
No response
Bits set:
INV & BCST to "1" in TW

BROADCAST WITHOUT DATA WORD
No response
Bits set:

5.2.16 OVERRIDE SELECTED TRANSMITTER SHUTDOWN (10101; T/R=0)

VALID COMMAND
Responds with status except if broadcast.
Bits set:
If broadcast- BCR, BCST to "1" in TW & SW.

COMMAND + EXTRA DATA WORD
No response
Bits set:
INV to "1" in TW.

COMMAND WITHOUT DATA WORD
No response
Bits set:

BROADCAST WITH EXTRA DATA WORD
No response
Bits set:
INV & BCST to "1" in TW

BROADCAST WITHOUT DATA WORD
No response
Bits set:

5.2.17 RESERVED MODE CODES (10110-11111; T/R=1)

VALID COMMAND
Responds with status and data word.
Bits set: *MDCD to "0" in CDR.

COMMAND + DATA WORD
No response
Bits set: *MDCD to "0" in CDR. ME to "1" in SW.
INV to "1" in TW.

BROADCAST COMMAND
UNIMPLEMENTED COMMAND

BROADCAST COMMAND+DATA WORD
UNIMPLEMENTED COMMAND

5.2.18 RESERVED MODE CODES (10110-11111; T/R=0)

VALID COMMAND
Responds with status except if broadcast.
Bits set:
If broadcast- BCR, BCST to "1" in TW & SW.

COMMAND + EXTRA DATA WORD
No response
Bits set:
INV to "1" in TW.

COMMAND WITHOUT DATA WORD
No response
Bits set:

BROADCAST WITH EXTRA DATA WORD
No response
Bits set:
INV & BCST to "1" in TW

BROADCAST WITHOUT DATA WORD
No response
Bits set:

6.0.0 INITIALIZATION

There are several types of initialization that can set up the NHI-ET parameters.

6.1.0 INTERNAL INITIALIZATION

There are two methods of initializing the NHI_ET. Each will produce the same results. They are: Hardware(MRST) and Software (writing to address 15, data not used). After these resets have been performed, the NHI_ET is set to the RT mode and all internal state machines are reset.

The hardwire terminal address is loaded when a harware or software reset occurs. The hardwire address is connected to I/O DAT(5:0) pins. I/O DAT(4:0) are used for the address and I/O DAT5 is used to set odd parity in the address. The address is wired using external 4.7K pull-down resistors to set a low and internal 64K pull-up resistors to set a high.

The following table summarizes the condition of internal registers after a reset has been performed.

REGISTER RESET TABLE

REGISTER	BITS=1	BITS=0	COMMENTS
CONTROL	HWD	ALL OTHERS	RT MODE INITIALIZED WITH TAG WORD
POINTER ADDRESS	-	-	LOADED WITH 2048 DECIMAL WORD
BASIC STATUS	*	ALL OTHERS	TADR FIELD GETS HARDWIRE ADDRESS
CONFIG REG 3	-	-	0008H
INT MASK	ALL	-	**ALL INTERRUPTS MASKED**
INT VEC	-	-	FFFFH
INT REQ	-	ALL	0000H
AUX VEC	-	-	UNDEFINED
RTC; HIGH-LOW	-	ALL	RTC RESET TO 0
RTC CONTROL	-	ALL	UPDATES IN BYTE MODE
FIFO	-	-	RESET AND CLEARED
LAST COMMAND	-	-	UNDEFINED
LAST STATUS	*	ALL OTHERS	TADR FIELD GETS HARDWIRE ADDRESS
ENCODER STATUS	-	ALL	0000H
CONDITION	ALL	-	FFFFH
FRAME "A" POINTER	-	-	LOADED WITH 2048 DECIMAL WORD
FRAME "B" POINTER	-	-	LOADED WITH 4096 DECIMAL
FRAME "A" ADDRESS	-	-	0800H
FRAME "B" ADDRESS	-	-	1000H
MSG MONITOR ADDRESS FILTER 1	-	ALL	0000H
MSG MONITOR ADDRESS FILTER 2	-	ALL	0000H

* See RESET BUSY TABLE

RESET FUNCTION TABLE

RESET TYPE	REGISTERS	STATE MACHINES
Mode Code Reset	No Change	No Change
Hardware Reset(MRST)	Reset	Reset
Software Reset	No Change	Reset

RESET BUSY TABLE

RESET TYPE	RTCC_6	CNFG1_1	BUSY BIT
HARDWARE(MRST)	X	X	SET
SOFTWARE	0	0	SET
SOFTWARE	X	1	No Change
SOFTWARE	1	X	No Change
MODE CODE 8	0	0	SET
MODE CODE 8	1	X	No Change
MODE CODE 8	X	1	No Change

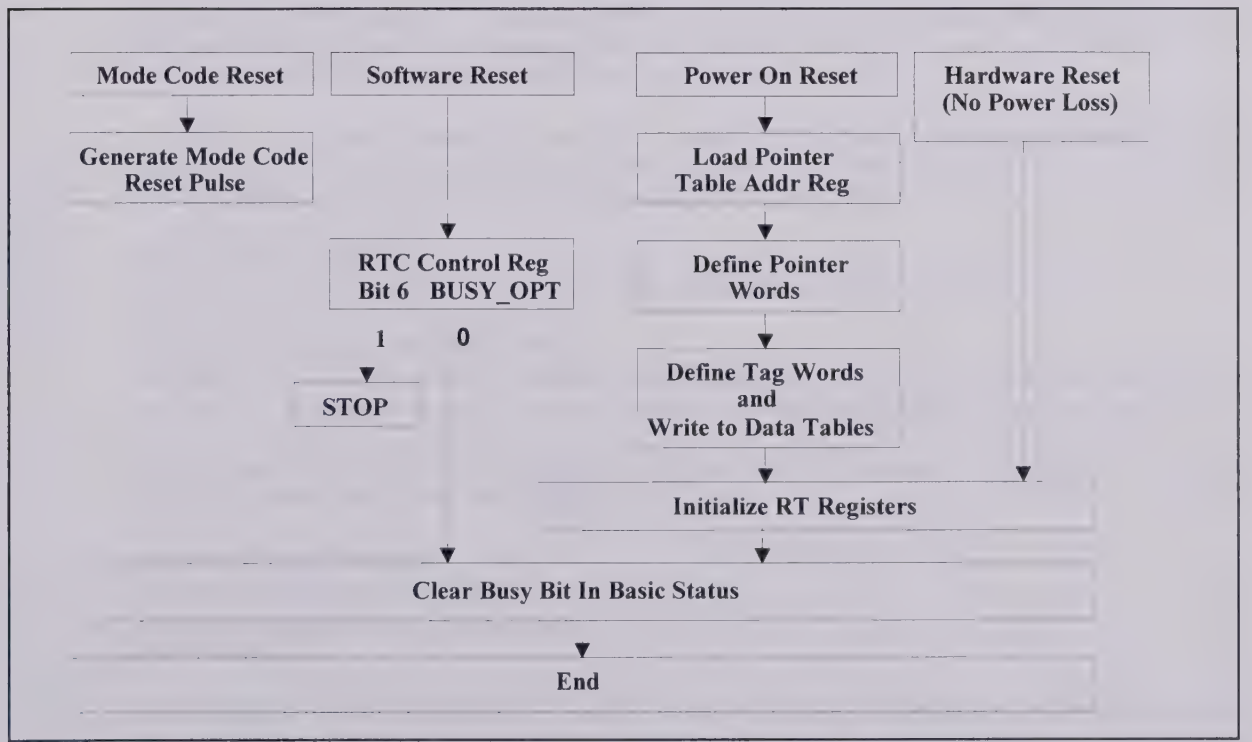
The RAM is not initialized or reset by any of the internal initialization routines performed by the ET. The pointer tables and data tables are not defined.

6.2.0 HOST INITIALIZATION OF NHI-ET

The host will usually want to initialize the ET at power up or at any other time it feels the procedure is necessary. At power up the host must initialize the registers discussed in the preceding section if the default settings of the internal initialization are not suitable. In addition the host must initialize the RAM, the pointer tables, and the data table tag words for each command type and subaddress.

The host initialization of the registers is also required only after a hardware reset. Since the RAM is not affected by any resets, it does not have to be re-initialized unless data has been lost or corrupted, therefore the pointer tables will remain intact.

The following flow diagram is a suggested method of host initialization of the NHI-ET in the RT mode as a function of the type of reset which has occurred.



7.0.0 INTERRUPT HANDLING

When an interrupt request is received by the NHI- ET, the *IRQ line goes low and header information about

the message that caused the interrupt is pushed on an internal FIFO. If another interrupt request is received before the CPU performs an acknowledge, it's header information is also pushed onto the FIFO. In this manner, there is no danger of losing interrupt vectors or header information due to receiving multiple interrupt requests before an acknowledge by the CPU takes place. The FIFO can hold header information for six interrupt messages. If an interrupt request occurs when the FIFO is full, a vector indicating FIFO overflow is first pushed onto the FIFO and then the header information for the message which caused the overflow is pushed onto the FIFO. As a result, the header information from the two oldest messages is lost.

If the FIFO is in the revolving mode, the FIFO will store seven interrupts. When another interrupt is issued and the FIFO contains seven previous headers, the new header is pushed onto the FIFO and the oldest header is lost.

7.1.0 HARDWARE INTERRUPT ACKNOWLEDGE

To acknowledge an interrupt in hardware, the *INTACK line is taken low, the *HCS line held high and the *INTPI line is held low. This pops the interrupt header information off the FIFO and into the IVR and AVR. The *IRQ line will go high if the FIFO is empty, but remain low if there are additional interrupt headers on the FIFO. If the NHI-ET is in the RT mode, the IVR will be outputted on the upper and lower byte of the CPU data bus. If the *INTPI line is high, then *INTACK is ignored.

The IVR and AVR can be read from address 4 after performing the hardware interrupt.

If there are more interrupt headers on the FIFO, indicated by the *IRQ remaining low after the interrupt acknowledge, the procedure is repeated until the FIFO is empty. An empty FIFO is indicated by the *IRQ line returning high after an interrupt acknowledge and bit 8 in the AVR will be a "1".

7.2.0 SOFTWARE INTERRUPT ACKNOWLEDGE

If the host CPU does not support a hardware interrupt acknowledge, a software acknowledge can be performed by reading address 8. This read pops the interrupt header information off the FIFO and into the IVR and AVR and places their contents on the CPU data bus. The *IRQ line will go high if the FIFO is empty and remain low if there are additional interrupt headers on the FIFO.

If there are more interrupt headers on the FIFO, indicated by the *IRQ remaining low after the interrupt acknowledge, the procedure is repeated until the FIFO is empty. An empty FIFO is indicated by the *IRQ line returning high after an interrupt acknowledge and bit 8 in the AVR will be a "1".

8.0.0 TIPS - HINTS 'N TRICKS

This section will help the USER to apply the ET to a system and implement its various features.

8.1.0 BUS CONTROLLER APPLICATIONS

The NHI-1582ET Bus Controller is flexible, powerful, and very easy to use. The number of operations required to initialize the device and to examine results of a data message transfer has been minimized.

The BC function of the NHI-1582ET employs registers embedded in the protocol chip and its internal ram to perform its various tasks. These tasks include:

Initiating Message Transfers
Diagnose RT Responses
Take Appropriate Action on Error Conditions
Data Storage

Message lists, containing the addresses of specific messages, are used to develop specific operational scenarios. The number of message lists and message tables is limited only by the size of the ram. A list can have up to 1024 messages. A message list is activated by placing its address in one of the two FRAME START REGISTERS and the list length in one of the FRAME LENGTH REGISTERS.

8.1.1 BC REGISTERS

This a brief description of the BC registers and their role. Specific bit functions are given in the address map section of this manual. Only the functions pertinent to the BC are described here. The following registers are used in the BC function:

8.1.1.1 CONFIGURATION REG 2 Address: 4

8.1.1.1.1 Complete EOM and continue.

8.1.1.1.2 Goto next message.

8.1.1.1.3 Goto EOF and continue.

8.1.1.1.4 Stop at end of current message.

8.1.1.1.5 Stop at end of current frame.

8.1.1.1.6 Abort - Go off line.

8.1.1.1.7 Go default frame.

Note: Functions 1,2 and 3 only apply to a bus jam condition.

8.1.1.2 CONFIGURATION REG 1 Address: 9

8.1.1.2.1 Mode select - RT, BC, MT.

8.1.1.2.2 Start BC.

8.1.1.2.3 Select default frame A or B.

8.1.1.2.4 Select default bus A or B.

8.1.1.2.5 Force bus A or B.

8.1.1.3 FRAME "A" POINTER Address: 13

8.1.1.3.1 Holds address of a selected BC message list.

8.1.1.4 FRAME "A" LENGTH Address: 14

8.1.1.4.1 Holds number of messages in frame A message list.

8.1.1.4.2 End of frame A options - Stop, Repeat , Go Alternate.

8.1.1.4.3 Stop on frame error.

8.1.1.4.4 Stop on status set.

8.1.1.4.5 Interrupt at end of frame.

8.1.1.5 FRAME "B" POINTER Address: 16

8.1.1.5.1 Holds address of a selected BC message list

8.1.1.6 FRAME "B" LENGTH Address: 17

8.1.1.6.1 Holds number of messages in frame B message list.

8.1.1.6.2 End of frame B options - Stop, Repeat, Go Alternate.

8.1.1.6.3 Stop on frame error.

8.1.1.6.4 Stop on status set.

8.1.1.6.5 Interrupt at end of frame.

8.1.1.7 CONDITION REGISTER Address: 19

8.1.1.7.1 Bus A jammed.

8.1.1.7.2 Bus B jammed.

8.1.1.7.3 Current BC frame A or B.

8.1.1.7.4 End of frame A.

8.1.1.7.5 End of frame B.

8.1.1.7.6 Current frame busy.

8.1.1.8 **END OF FRAME GAP** Address: 20

8.1.1.8.1 End of frame delay before start of next frame - 64us resolution, 16 bits.

8.1.1.9 **CONFIGURATION REG 3** Address: 21

8.1.1.9.1 Sets bus jam threshold - the number of extra words(0- 31) a message can have before a bus jam is declared.

8.1.1.9.2 Defines response to BCST bit if set in status word.

8.1.1.9.3 Sets global retry options.

8.1.2 **BC RAM**

The BC ram is used to store message lists and message tables. A message list is a block of consecutive memory locations, each of which contains the address of a message table. This list can contain any number of message table addresses up to a maximum of 1024. Many message lists can be stored in the ram, limited only by ram size, each one containing a different scenario. A particular message table may be a member of any number of message lists and occupy the same or different positions in each list.

8.1.3 **BC MESSAGE TABLE**

A message table is a block of consecutive memory which contains all the components of one message. These components are:

8.1.3.1 BC Control word.
8.1.3.2 BC Command word.
8.1.3.3 Message gap word.
8.1.3.4 32 bit time tag(two words).
8.1.3.5 2nd Command word (RT-RT only).
8.1.3.6 Data words.
8.1.3.7 Status word.
8.1.3.8 2nd Status word(RT-RT only).

In the case of an RT-RT transfer, the second command and status words are also in the message block as shown. The message block is designed to contain all the information associated with the message. Parts of the message, the command word for example, are not segregated into a separate ram area which would complicate reading or writing a message block by the CPU. The unified message block approach used in the NHI-1582ET provides faster access to a message block by the CPU and minimizes overhead.

8.1.4 **BC CONTROL WORD**

The BC control word is used by the CPU to define parameters in the message and it is used by the Protocol chip to report information back to the CPU. The following parameters are loaded into the BC control word by the CPU and used by the protocol chip for a message:

8.1.4.1 Status bit analysis.
8.1.4.2 Message bus - A or B.
8.1.4.3 Local retry actio in the event of an error. If there is no local retry, then the global retry action set in configuration register 2 is used if an error occurs.

The following information about that message is loaded into the BC control word by the protocol chip and used by the CPU:

8.1.4.4 Start of message flag.
8.1.4.5 No response.
8.1.4.6 Error.
8.1.4.7 Status bit set.
8.1.4.8 Retry attempted.
8.1.4.9 End of message flag.

8.1.5 BC COMMAND WORD

The command word is any of the 1553 valid commands. This word defines the type of data transfer in the message BC to RT, RT to BC, RT to RT, or Mode code.

8.1.6 MESSAGE GAP WORD

The message gap word defines delay between the end of the current message and the start of the next message in the list. The maximum intermessage gap is 4ms with a resolution 1us. The minimum inter message gap is approximately 8us when the delay is set to 0. The following other parameters are set in the message gap word:

8.1.6.1 Message stop on error.
8.1.6.2 Message stop on status set.
8.1.6.3 Interrupt on end of message.
8.1.6.4 NO-OP.

If the NO-OP is set in a message, the message is ignored except for its inter message delay. This feature can be used to extend the maximum intermessage gap from 4ms to any length, just by putting a series of NO-OP messages between two operational messages.

8.1.7 32 BIT TIME TAG(2 WORDS)

The internal time tag resolution is selectable as 1,2,4,8,16,32 or 64us.

8.1.8 BC INTERRUPTS

The following conditions will cause an interrupt to the CPU if they are not masked by the interrupt mask register.

PRIORITY	INTERRUPT	COMMENT
0	End of Message	Enabled in Msg Gap word
1	End of Frame	Enabled in Reg 14 & 17
2	Error	The RT response contained one or more errors.
3	Retry	The message was retried due to an RT error.
4	Fifo Over Flow	The FIFO is full.
5	Status Set	One or more status bits set; or status address error.
6	No Response	The RT did not responed
7	Failsafe Time Out	A Failsafe time out occurred in the ET's encoder.

The following header information about the BC message that caused the interrupt is pushed on to the Fifo:

8.1.8.1 Priority
8.1.8.2 Message number in frame
8.1.8.3 Frame A or B
8.1.8.4 Bus A or B

8.1.8.5 Fifo empty

8.1.9 BUS CONTROLLER EXAMPLES

Now, lets see how we would put the BC into operation!

The following sequence is one approach:

8.1.9.1 Define various message tables and load them into ram.
8.1.9.2 Define various message lists and load them withn the addresses of the previously defined message tables.

At this point, we have the ram loaded with individual messages tables and a number of message lists. Each message list contains the addresses of several(up to 1024) message tables.

8.1.9.3 Load the address of the first message list to be used into register 13, Frame A.
8.1.9.4 Load the total number of messages in that list into register 14, Frame length A.
8.1.9.5 Load the address of the second message list to be used into register 16, Frame B.
8.1.9.6 Load the total number of messages in that list into register 17, Frame length B.
8.1.9.7 Set the mode to BC in register 9.
8.1.9.8 Set the default frame to A in register 9.
8.1.9.9 Set the "Default bus" in register 9.
8.1.9.10 Set "Go alternate frame" in register 14.
8.1.9.11 Set "int on EOF" in register 14.
8.1.9.12 Set "Stop at EOF" in register 17.
8.1.9.13 Set "int on EOF" in register 17.
8.1.9.14 Set "Start BC" in register 9.

Based on these setup conditions, the following events will occur:

Frame A will execute the message list it contains. At the end of frame A, a frame gap delay will occur if a number other than 0 was loaded into register 20. At the end of the frame gap delay, The alternate frame, in this case B, will execute the message list it contains. At the end of frame B, the sequence will end and the BC will go off line.

Note: The alternate frame is the frame which is NOT the current frame. If the current frame is B, then the alternate frame is A. The alternate bus is the bus which is NOT the active bus.

This method is applicable if each message list contains many messages, tens or hundreds; however, each message list may only contain 10 or 20 messages and we would like to run a number of the small message lists automatically.

For the case of running many small message lists automatically, the approach is slightly different.

Lets say we want to run 10 different message lists automatically.

First create a super message list which contains all the addresses of the 10 smaller sub message lists. If we want to know when each of the sublists is completed, set the last message in each sub list to fire the interrupt. If we want to examine some of the data before the next sub list begins, set the inter message gap on the last message of the sub list to what ever delay is required. Then:

8.1.9.15 Load the address of the super message list into register 13, Frame A.
8.1.9.16 Load the total number of messages in the super list into register 14, Frame length A.
8.1.9.17 Set the mode to BC in register 9.
8.1.9.18 Set the default frame to A in register 9.
8.1.9.19 Set the "Default bus" in register 9.
8.1.9.20 Set "int on EOF" in register 14.
8.1.9.21 Set "Stop at EOF" in register 14.
8.1.9.22 Set "Start BC" in register 9.

All the messages in the super list will be executed and an interrupt will be issued at the end of each sub list. An intermessage gap of some defined value will separate each sub list of messages.

Instead of stopping at the end of frame A, we could have elected to "Go alternate frame", in which case, frame B would then execute what ever message lists were in frame B. If we then selected the "Go alternate frame" option at the end of frame B, frame A would be executed.

Note: The default frame is the frame selected in configuration register 1.The default bus is the bus selected in the BC control word.

8.1.10 SAMPLE BUS CONTROLLER MEMORY MAP

BC Registers

REGISTERS	DATA(hex)
Configuration 1	0900
Configuration 2	0000
Configuration 3	0003
Interrupt Mask	0000
Frame A, Pointer Table Address	0100
Frame A, Length	0003

Frame "A" Pointers

Address	Description	Data
0100	Data Block Address MSG 1 (BC-RT 2 words)	0200
0101	Data Block Address MSG 2 (RT-BC 4 words)	0220
0102	Data Block Address MSG 3 (RT-RT 6 words)	0240
0103	Data Block Address MSG 4 (Broadcast 1 word)	0260

BC FRAME "A" MESSAGE LIST

Address	Description	Data	Event
0200	MESSAGE LIST, MSG1 BC Control Word	****	
0201	BC Receive Command Word	0822	
0202	MSG Gap Word	****	
0203	MSG Time Tag MS Word	****	
0204	MSG Time Tag LS Word	****	
0205	BC Data Word 1	1111	
0206	BC Data Word 2	2222	
0207	RT Status Word	0800	End of Message Interrupt?
w	w	w	w
0220	MESSAGE LIST, MSG2 BC Control Word	****	
0221	BC Transmit Command Word	0C24	
0222	MSG Gap Word	****	

0223	MSG Time Tag MS Word	****	
0224	MSG Time Tag LS Word	****	
0225	RT Status Word	0800	
0226	RT Data Word 1	1111	
0227	RT Data Word 2	2222	
0228	RT Data Word 3	3333	
0229	RT Data Word 4	4444	End of Message Interrupt?
w	w	w	w
0240	MESSAGE LIST, MSG3 BC Control Word	****	
0241	BC Receive Command Word	0826	
0242	MSG Gap Word	****	
0243	MSG Time Tag MS Word	****	
0244	MSG Time Tag LS Word	****	
0245	BC Transmit Command Word	1426	
0246	Transmitting RT Status Word	1000	
0247	RT Data Word 1	1111	
0248	RT Data Word 2	2222	
0249	RT Data Word 3	3333	
024A	RT Data Word 4	4444	
024B	RT Data Word 5	5555	
024C	RT Data Word 6	6666	
024D	Receiving RT Status Word	0800	End of Message Interrupt?
w	w	w	w
0260	MESSAGE LIST, MSG4 BC Control Word	****	
0261	BC Broadcast Command Word	F821	
0262	MSG Gap Word	****	
0263	MSG Time Tag MS Word	****	
0264	MSG Time Tag LS Word	****	
0265	BC Data Word 1	1111	End of Block Interrupt? Repeat Current Message Block? Start Message Block 2?
w	w	w	w

8.2.0 MESSAGE MONITOR APPLICATIONS

The NHI-1582ET Message Monitor operation is very similar to that of the Bus Controller . The number of operations required to initialize the device and to examine results of a data message transfer has been minimized.
Each message can have an associated tag word and/or an associated 32 bit time tag.

The Message Monitor function of the NHI-1582ET employs registers embedded in the protocol chip and its internal ram to perform its various tasks. These tasks include:

Store Bus Messages
Diagnose RT Responses
Data Storage

A Message list, containing the addresses of message tables, is used to keep track of the message which have

been monitored and stored.. The number of message lists and message tables is limited only by the size of the ram. A list can have up to 1024 messages. A message list is activated by placing its address in one of the two FRAME START REGISTERS and the list length in one of the FRAME LENGTH REGISTERS.

The CPU defines the address of the first message table in a message list. After the first message table has been stored in ram, the ET calculates the address in ram where the next message table will be stored and writes it into the next contiguous address in the message list. This process continues, the ET calculating and writing succeeding message table addresses until the frame length has been reached. The Message Monitor then performs the indicated End-of_Frame action.

8.2.1 MESSAGE MONITOR REGISTERS

This a brief description of the Message Monitor registers and their role. Specific bit functions are given in the address map section of this manual. Only the functions pertinent to the Message Monitor are described here.

8.2.1.1 CONFIGURATION REG 2 Address: 4

8.2.1.1.1 Stop at end of current message.
8.2.1.1.2 Stop at end of current frame.
8.2.1.1.3 Abort - Go off line.
8.2.1.1.4 Go default frame.

8.2.1.2 CONFIGURATION REG 1 Address: 9

8.2.1.2.1 Mode select - RT, BC, MT.
8.2.1.2.2 Start MT.
8.2.1.2.3 Select default frame A or B.
8.2.1.2.4 Select Message or Word monitor.

8.2.1.3 FRAME "A" POINTER Address: 13

8.2.1.3.1 Holds address of a selected MT message list.

8.2.1.4 FRAME "A" LENGTH Address: 14

8.2.1.4.1 Holds number of messages in frame A message list.
8.2.1.4.2 End of frame A options - Stop, Repeat , Go Alternate.
8.2.1.4.3 Interrupt at end of frame.

8.2.1.5 FRAME "B" POINTER Address: 16

8.2.1.5.1 Holds address of a selected MT message list.

8.2.1.6 FRAME "B" LENGTH Address: 17

Holds number of messages in frame B message list.
End of frame B options - Stop, Repeat, Go Alternate.
Interrupt at end of frame.

8.2.1.7 CONDITION REGISTER Address: 19

8.2.1.7.1 Current BC frame A or B.
8.2.1.7.2 End of frame A.
8.2.1.7.3 End of frame B.
8.2.1.7.4 Current frame busy.

8.2.1.8 CONFIGURATION REGISTER 3 Address: 21

8.2.1.8.1 Enable tag word option.
8.2.1.8.2 Enable time tag option.

8.2.1.9 ADDRESS FILTER (0-15) Address: 22

8.2.1.9.1 Masks terminal addresses 0 - 15.

8.2.1.9.2 A "1" will mask the address.

8.2.1.10 **ADDRESS FILTER (16-31)** Address: 26

8.2.1.10.1 Masks terminal addresses 16 - 31.

8.2.1.10.2 A "1" will mask the address.

8.2.2 **MESSAGE MONITOR RAM**

The Message Monitor ram is used to store message lists and message tables in much the same manner as the BC. A message list is a block of consecutive memory locations, each of which contains the address of a message table. This list can contain any number of message table addresses up to a maximum of 1024. Many message lists can be stored in the ram, limited only by ram size, each one containing a different scenario.

8.2.3 **MESSAGE MONITOR MESSAGE TABLE**

A message table is a block of consecutive memory which contains all the components of one message. These components include:

Tag word control word.
Command word or Status word.
32 bit time tag(two words).
Data words.

The format of a Message Table is a function of the type of command stored in ram. These formats are illustrated in a later section of this manual. The unified message block approach again used in the Message monitor to provide faster access to a message block by the CPU and minimizes overhead.

8.2.4 **MESSAGE MONITOR TAG WORD**

The ET loads the Message monitor tag word with information about the message received. This information is used by the CPU to analyze the message.

The following parameters are loaded into the Monitor tag word by the ET:

8.2.4.1 Start of message flag.

8.2.4.2 Data error - Data word(s) contained error(s).

8.2.4.3 Command 1 error - Comand word contained error(s).

8.2.4.4 Command 2 error - Second command word of an RT-RT command contained error(s).

8.2.4.5 Over lap - A message was detected on the alternate bus before the current message was completed The Message monitor aborts processing the current message, switches to the alternate bus and begins processing the new message.

8.2.4.6 Sync error - A contiguous data word had a command sync.

8.2.4.7 Bus A-B.

8.2.4.8 RT-RTcommand - Message was an RT-RT command.

8.2.4.9 End of message flag.

8.2.5 **COMMAND WORD OR STATUS WORD**

This is the Command or Status word associated with the message.

8.2.6 **DATA WORD(S)**

These are the data word(s) associated with the message.

8.2.7 **MESSAGE MONITOR EXAMPLE**

Setting up and Implementing the MESSAGE monitor!

8.2.7.1 Put address of message list in FRAME REG.

8.2.7.2 Put address of 1st message table in 1st location of message list.

8.2.7.3 Put message list size in FRAME LENGTH REG.

8.2.7.4 Set end of MESSAGE LIST options in FRAME LENGTH REG.
8.2.7.5 Select end of MESSAGE LIST interrupt in FRAME LENGTH REG.
8.2.7.6 Set the address Masks in REG's 22 and 26.
8.2.7.7 Select tag word option in REG 21.
8.2.7.8 Select time tag option in REG 21.
8.2.7.9 Select MESSAGE monitor in REG 9.
8.2.7.10 Start monitor in REG 9.

The monitor now collects messages until the message list size is reached. The selected End-of-Message List option is executed and an interrupt is issued if enabled.

The CPU can now read the entire message list. Each word in the message list is the address of a data block stored in ram. The first word in the block is the Tag Word associated with that message.

8.3.0 WORD MONITOR APPLICATIONS

The NHI-1582ET Word Monitor operation collects dtat on a word-by-word basis . Each word that is received and stored in the ram can have an associated tag word and/or an associated 32 bit time tagged The number of operations required to initialize the device and to examine results of a data message transfer has been minimized.

The Word Monitor function of the NHI-1582ET employs registers embedded in the protocol chip and its internal ram to perform its various tasks. These tasks include:

Store Bus words
Diagnose RT Responses
Data Storage

A data block, containing the bus word ,tag word and time tag, is used to store the monitored data.. The begining of the data block is determined by the address placed in the BLOCK START REGISTER and the end of the data block is determined by the address in the BLOCK END REGISTER.

The BLOCK END REGISTER works inconjunction with the LAST ADDRESS REGISTER. Since a bus word can occupy up to four words in ram, tag word + 2 time tag words, the address in the BLOCK END REGISTER could occur on any of these four words. In order to keep the four words of the last ram entry contiguous in ram, the Word monitor uses the LAST ADDRESS REGISTER to store the address of the last word in the data block. The ET calculates this address and puts it in the LAST ADDRESS REGISTER. This address could be identical the that in the BLOCK END REGISTER or up to three addresses greater; therefore, always reserve the four addresses after the address in the BLOCK END REGISTER for this contingency.

8.3.1 WORD MONITOR REGISTERS

This a brief description of the Message Monitor registers and their role. Specific bit functions are given in the address map section of this manual. Only the functions pertinent to the Message Monitor are described here.

8.3.1.1 CONFIGURATION REG 2 Address: 4
8.3.1.1.1 Stop at end of current message.
8.3.1.1.2 Stop at end of current frame.
8.3.1.1.3 Abort - Go off line.
8.3.1.1.4 Go default frame.

8.3.1.2 CONFIGURATION REG 1 Address: 9
8.3.1.2.1 Mode select - RT, BC, MT.
8.3.1.2.2 Start MT.

8.3.1.2.3 Select default frame A or B.
8.3.1.2.4 Select Message or Word monitor.

8.3.1.3 **BLOCK "A" START** Address: 13
8.3.1.3.1 Holds address of a selected MT message list.

8.3.1.4 **BLOCK "A" END** Address: 14
8.3.1.4.1 Holds number of messages in frame A message list.
8.3.1.4.2 End of frame A options - Stop, Repeat , Go Alternate.
8.3.1.4.3 Interrupt at end of frame.

8.3.1.5 **BLOCK "B" START** Address: 16
8.3.1.5.1 Holds address of a selected MT message list.

8.3.1.6 **BLOCK "B" END** Address: 17
8.3.1.6.1 Holds number of messages in frame B message list.
8.3.1.6.2 End of frame B options - Stop, Repeat , Go Alternate.
8.3.1.6.3 Interrupt at end of frame.

8.3.1.7 **CONDITION REGISTER** Address: 19
8.3.1.7.1 Current BC frame A or B.
8.3.1.7.2 End of frame A.
8.3.1.7.3 End of frame B.
8.3.1.7.4 Current frame busy.

8.3.1.8 **WORD MONITOR END OF BLOCK OPTIONS** Address: 20
8.3.1.8.1 End of block A options - Stop, Repeat, Go Alternate.
8.3.1.8.2 Interrupt at end of block A.
8.3.1.8.3 End of block B options - Stop, Repeat, Go Alternate.
8.3.1.8.4 Interrupt at end of block B.

Address: 21

8.3.1.9 **CONFIGURATION REGISTER 3**
8.3.1.9.1 Enable tag word option.
8.3.1.9.2 Enable time tag option.
8.3.1.9.3 Enable time tag command syncs only option.

8.3.2 **WORD MONITOR EXAMPLE**

Setting up and Implementing the WORD monitor!

8.3.2.1 Set address of data block in BLOCK A/B REG.
8.3.2.2 Set end of data block address in BLOCK A/B END REG.
8.3.2.3 Set end of DATA BLOCK options in REG 20.
8.3.2.4 Select end of block interrupt in REG 20.
8.3.2.5 Select tag word option in REG 21.
8.3.2.6 Select time tag option in REG 21.
8.3.2.7 Select word monitor in REG 9.
8.3.2.8 Start monitor in REG 9.

The monitor now collects data until the end of block address is reached. The address of the last word in the block is stored in the Last Word Address register, the selected End-of-Block option is executed and an end of block interrupt is issued if enabled in reg 20.

The CPU can now read the entire data block and use the Tag Words and the Time Tags to analyze the data.

8.4.0 **SIMULTANEOUS MONITOR AND REMOTE TERMINAL**

The ET can operate as a simultaneous monitor and remote terminal. This mode is activated by setting bits 8 and 9 of Configuration register 1 to a "1". In this mode the ET will respond as a remote terminal to the address set in the Basic Status register. This address is set either by the hardwire address or software.

The ET will respond to all addresses except that in the Basic Status register as a monitor, word monitor or message monitor depending on the monitor mode selected. In the message monitor mode, the ET will only respond to terminal addresses which **have not** been masked in registers 22 and 26.

When the ET receives a message with the address in the Basic Status register, it will become a fully operational Remote Terminal for that message.

8.4.1 SIMULTANEOUS MODE INTERRUPT HANDLING

In this dual mode of operation, all the interrupts for the Remote terminal and Monitor operation remain valid; therefore both RT and MT messages can set interrupts and push headers on the FIFO during the dual mode operation.

When an interrupt is pushed on the FIFO, the priority level determines the circumstances that caused it. See the AVR and IVR descriptions for details. The following table describes the type of message which issued the interrupt in the Simultaneous mode:

PRIORITY LEVEL	MESSAGE TYPE
1, 2, 3, 7	Remote Terminal
5	Monitor
4	Fifo Overflow

8.5.0 PC BOARD CONSIDERATIONS AND GUIDE LINES

8.5.1 There are a few guide lines which should be observed when mounting the ET and its coupling transformer on a PC board. The following considerations will prevent layout problems on the board:

8.5.1.1 The width of the two land traces for each Bus from the ET to the transformer must be as wide as possible(0.1in min width).

8.5.1.2 The length of the two land traces for each Bus from the ET to the transformer must be as short as possible(0.5in max length).

8.5.1.3 The two land traces for each Bus from the ET to the transformer must be balanced in length and width.

8.5.1.4 There should be no ground plane or power plane under the ET, the transformer or the land traces connecting the transformer to the ET.

8.5.1.5 The center tap of the transformer primary must be connected to ground with a heavy short land trace.

8.5.1.6 The center tap of the transformer secondary should be left floating.

8.5.1.7 All the power and ground pins on the ET must be connected.

8.5.1.8 A 0.1uf capacitor should be connected from each power pin on the ET to ground.

9.0.0 PIN FUNCTIONAL DESCRIPTION

The NHI-ET I/O pins are divided into 5 families:

General purpose signals
Host interface signals
I/O bus interface signals
1553 interface signals
Power

9.1.0 GENERAL PURPOSE SIGNALS

9.1.1 MRST_L

RST_L=0 (active low, input).
Initializes all registers and state machines. ET reads hardwire terminal address.

9.1.2 CLK_H

Clock from 10 Mhz oscillator (input).

9.2.0 HOST INTERFACE IGNALS

9.2.1 H_DAT (15:0)

HOST DATA bus (bi-directional).

9.2.2 H_ADR(14:1)

HOST ADDRESS bus (input).

9.2.3 HCS_L

CHIP SELECT (active low, input).
Selects the NHI-ET. The falling edge of HCS_L is used to latch the host's address and indicates the start of a host memory cycle. The rising edge terminates the current cycle. During a host read-modify-write cycle, this signal must remain active from the beginning of the read cycle to the end of the write cycle.
NOTE: The host should not hold *HCS active for more than 5 microseconds, otherwise timing errors on the 1553 bus may occur.

9.2.4 HWRL_L

HOST WRITE LOWER BYTE (active low, input).

9.2.5 HWRH_L

HOST WRITE UPPER BYTE (active low, input).

9.2.6 HRD_L

HOST READ (active low, input).

9.2.7 DTACK_L

HOST DATA TRANSFER ACKNOWLEDGE (active low, open drain output). Indicates to the host that a data transfer has been completed. When the host reads data, it takes HCS_L low and the HRD_L low. The ET then indicates that able data is on the bus by outputting a low on DTACK_L. When the host writes data, it takes HCS_L low and then HWRL_L and/or HWRH_L low. The ET then indicates that it has completed the write cycle by outputting a low on DTACK_L.

9.2.8 IRQ_L

Host INTERRUPT REQUEST (active low, open drain output).

9.2.9 INTACK_L

Host INTERRUPT ACKNOWLEDGE (active low, input).
Indicates that the host is acknowledging an interrupt. When HRD_L=0, INTACK_L=0, and HCS_L=1, an interrupt vector is popped from the FIFO, the IVR/AVR registers are updated, and the IVR is outputted onto both the lower and upper bytes of the host data bus provided that the INTPI_L is low (see *INTPI description) and the ET is in the RT mode.

9.2.10 **INTPI_L**

INTERRUPT PRIORITY INPUT (active low, input).
This signal is used to daisy chain interrupt requests on the host bus. This signal must be active for the ET to output an interrupt vector.

9.2.11 **IPO_L_DSC**

INTERRUPT PRIORITY OUTPUT, DISCONNECT SIGNAL (output).

This pin has 2 possible functions, depending on the M1760 bit in the RTC CONTROL register.

If M1760=0, then the signal is used to daisy chain interrupt requests on the host bus. When the ET requests an interrupt, this signal is output high; otherwise, this signal is equal to INTPI_L.

If M1760=1, then the pin is set to "1" when the store is disconnected (see EXTERNAL TERMINAL ADDRESS BUFFER for details).

9.3 DISCRETE I/O BUS INTERFACE SIGNALS

9.3.1 **I/O_RD_L**

I/O READ (active low, output).

9.3.2 **I/O_WR_L**

I/O WRITE (active low, output).

9.3.3 **I/O_ADR (2:1)**

I/O ADDRESS (outputs).
These signals can be used to select 4 byte-wide input devices and 4 byte-wide output devices which reside on the I/O bus.

9.3.4 **I/O_DAT (7:0)**

I/O DATA bus (bi-directional).

9.3.5 **CMDS**

STROBE (active high, output).
This strobe is used for two special I/O operations. When the strobe is active during a write cycle (i.e., CMDS=1, I/O WR_L=0), valid commands/pulses appear on the I/O bus (see the CMDO bit in CONTROL register for details). When the strobe is active during a read cycle (i.e., CMDS=1, I/O RD_L=0), the EXTERNAL TERMINAL ADDRESS buffer is accessed.

9.3.6 **PLSCMD_BUS_JAM**

PULSE COMMAND or BUS JAM (active high, output).
RT MODE:
Depends on the value of the CMDO bit in the CONTROL register. If CMDO=0, then a pulse is issued whenever a 1553 message accesses a data table with PULSE (3:0)=14 (decimal) in its tag word. If CMDO=1, then a pulse is issued whenever a valid broadcast command is received.

Note: The NTAG bit in the CONTROL register must be 0 to get a pulse output.

BC MODE:
This pin will go high and the BC will halt if a bus jam occurs. The CPU must then intervene to allow the BC to continue processing the frame (See configuration register 2 for details).

MDCDRST

MODE COMMAND RESET (active high, 400 nS pulse, output).
Pulsed high whenever a mode command "Reset" is received in the RT mode.

SSF_TF SUBSYSTEM FLAG, TERMINAL FLAG (active high, input). Sets either the SUBSYSTEM FLAG bit or the TERMINAL FLAG bit in the STATUS register. The SSF_TF bit in the CONTROL register determines which status bit will be set by this input (see CONTROL register for details).

9.4 MIL-STD-1553B INTERFACE SIGNALS

BUS_A, BUS_A_L 1553 BUS A signals (bi-directional). Connected to a bus coupling transformer.

BUS_B, BUS_B_L 1553 BUS B signals (bi-directional). Connected to a bus coupling transformer.

TXINH_A BUS A INHIBIT (input). Inhibits the bus A transmitter.

TXINH_B BUS B INHIBIT (input). Inhibits the bus B transmitter.

10.0.0 ELECTRICAL CHARACTERISTICS

10.1.0 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units	Remarks
DC Supply voltage	VCC	-0.3	+7	Volts	
Input voltage	VIN	-0.3	VCC+0.3	Volts	Note 1
DC Input current	IIN	-10	10	Microamps	Note 2
Input zapping	VZAPP	2,000		Volts	Note 3
Latch-up trigger current	ILATCH		200	Milliamps	Note 4
Thermal resistance	Θ jc		4	°C/W	
Storage temperature	Tstorage	-65	150	°C	
Lead temperature	TL		300	°C	

Note 1: VCC referenced to ground
Note 2: Does not include current through internal 64K ohm pull-up/down resistors.
Note 3: As defined for ESDS in Method 3015 0f MIL-STD-883.
Note 4: The latch-up triggering current is the maximum current that will not cause latch-up on an I/O BUFFER.

10.2.0 OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Units
Supply voltage	VCC	4.5	+5.5	Volts
Supply current	ICC			
0% TX duty-cycle			90	Milliamps
100% TX duty-cycle			675	Milliamps
Output level on bus	Vpp	7.1	9	Volts
Output level on Stub	Vpp	20	27	Volts
Ambient operating temperature range	TA	-55	+125	°C

10.3.0 I/O TYPES & DESCRIPTIONS

I/O TYPES	DESCRIPTION
1	Bi-directional 3-state buffer with 64K ohm pull-up
2	Bi-directional 3-state buffer with 64K ohm pull-up
3	Output Buffer
4	Output Buffer
5	Open-drain Output Buffer
6	Input Buffer with 64K ohm pull-up
7	Input Buffer with 64K ohm pull-down
8	Input Buffer

Signal Name	I/O	Signal Name	I/O	Signal Name	I/O	Signal Name	I/O
H_DAT(15:0)	1	DSC_INTPO_L CMDS	3	DTACK_L IRQ_L	5	CLK10	7
I/O_DAT(7:0) I/O_ADR(2:1)	2	MDCDRST PLSCMD I/O_RD_L I/O_WR_L	4	H_ADR(14:1) HRD_L HWRL_L HWRH_L HCS_L RST_L INTPI_L INTACK_L SSF_TF	6	TXINH_A TXINH_B	8

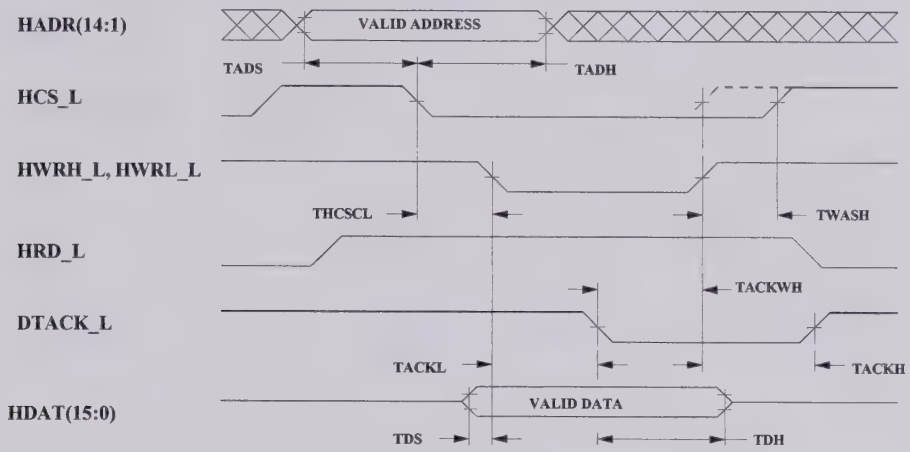
10.4.0 I/O ELECTRICAL CHARACTERISTICS

Parameter	I/O Type	Condition	Min	Max	Units
Low-level input voltage	1,2,6,7,8			0.8	Volts
High-level input voltage	1,2,6,7,8		2		Volts
Low-level output voltage	1	IOL < 8.0 ma		0.4	Volts
	2	IOL < 4.0 ma		0.4	Volts
	3	IOL < 4.0 ma		0.4	Volts
	4	IOL < 6.0 ma		0.4	Volts
	5	IOL < 16.0 ma		0.4	Volts
High-level output voltage	1	IOH > -8.0 ma	2.4		Volts
	2	IOH > -4.0 ma	2.4		Volts
	3	IOH > -4.0 ma	2.4		Volts
	4	IOH > -6.0 ma	2.4		Volts
Input Cap.				10	PF

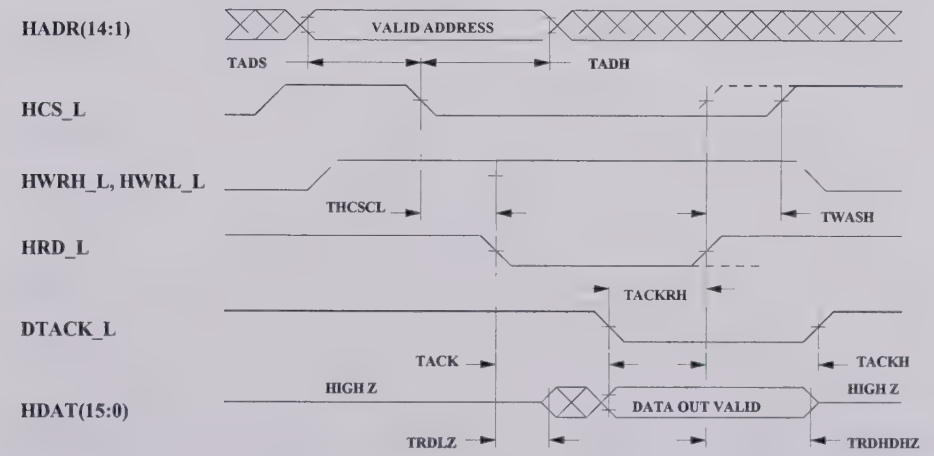
11.0.0 TIMING DIAGRAMS

The following diagrams and notes describe the timing of the address, data, and control lines.

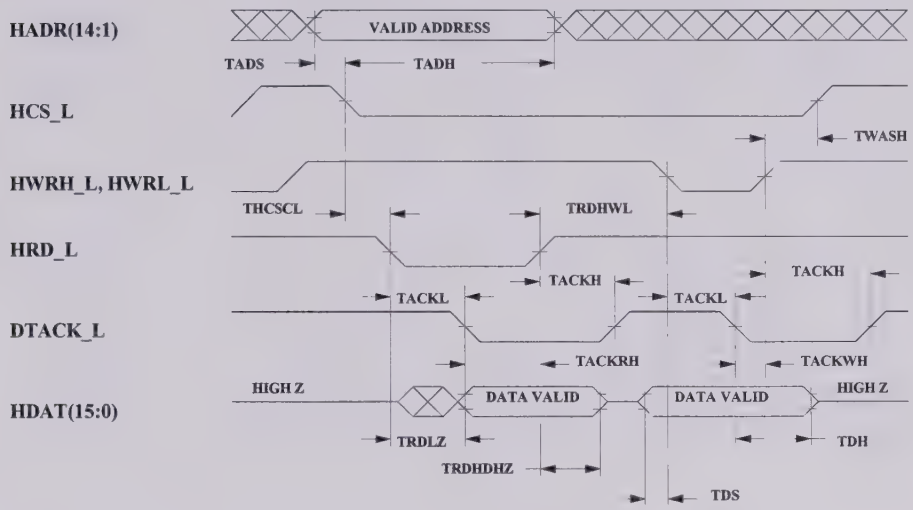
11.0.1 HOST WRITE CYCLE



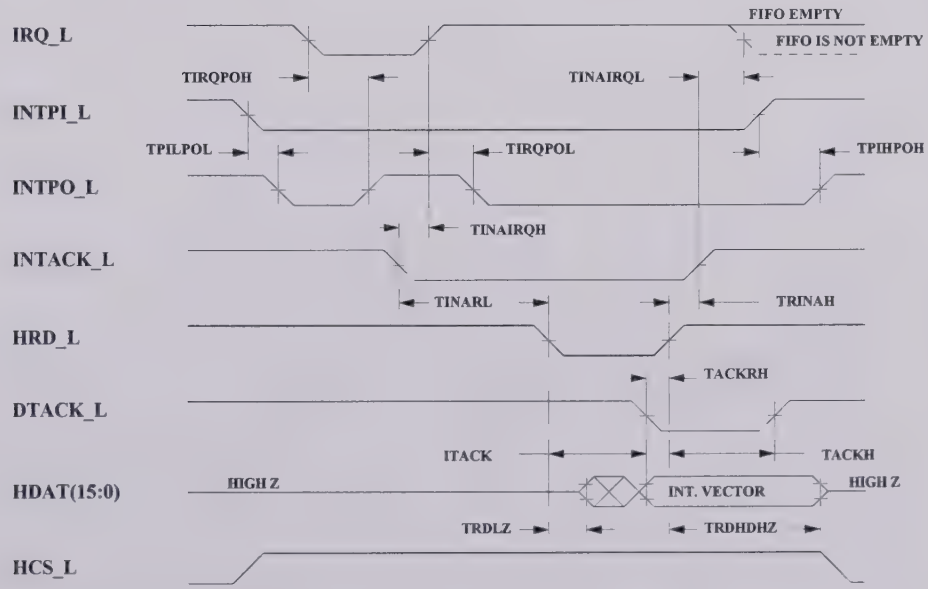
11.0.2 HOST READ CYCLE



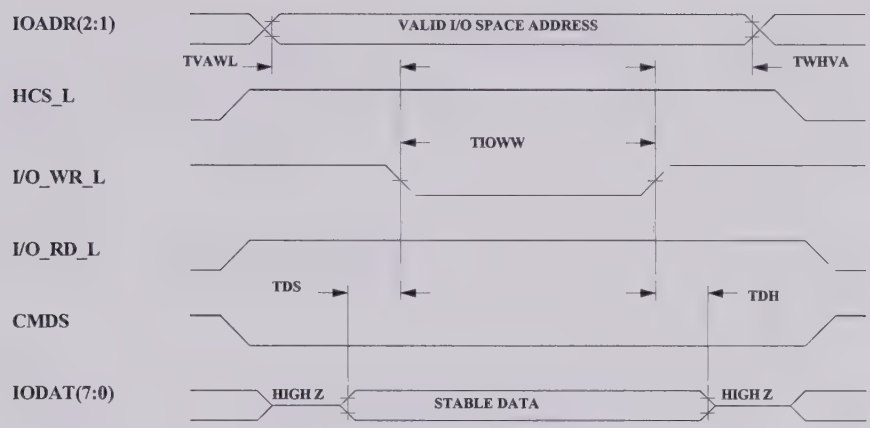
11.0.3 HOST READ-MODIFY-WRITE CYCLE



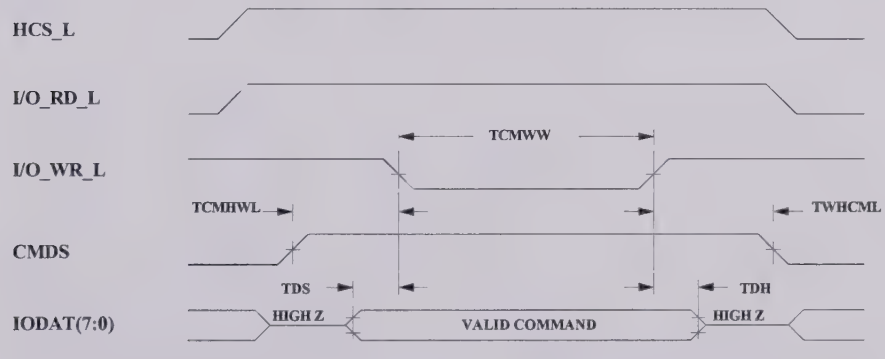
11.0.4 INTERRUPT ACKNOWLEDGE CYCLE



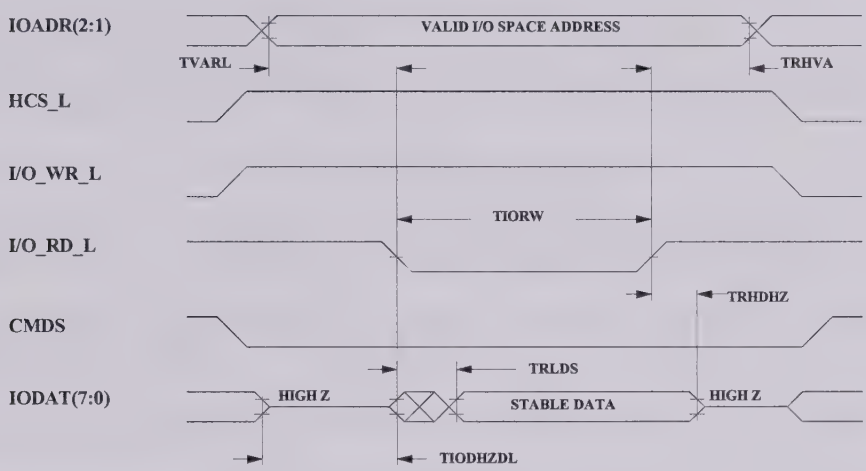
11.0.5 I/O WRITE CYCLE



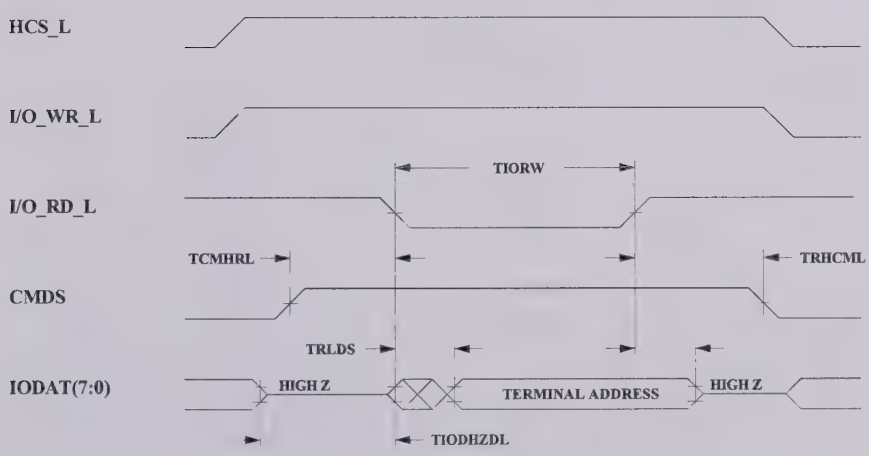
11.0.6 COMMAND WRITE CYCLE



11.0.7 I/O READ CYCLE



11.0.8 TERMINAL ADDRESS READ CYCLE



11.0.9 TIMING NOTES

The address is latched by the NH-ET on the high-to-low transition of the *HCS line. TADS, TADH, and TASLC are referenced to the high-to-low transition of *HCS.

TACK is a function of the contending access performed by the NHI-ET (see host access table).

The low-to-high transition of *HRD or I/O *RD terminates the read cycle.

The *DTACK line is tri-stated after delay TACKH. Its rise time is a function of the internal 5K ohm pull-up resistor and the external load.

While *INTACK is low, *INTPO will be affected by changes in *IRQ.

In order to support edge triggered interrupt requests, *IRQ is returned high TINAIRQH ns after *INTACK goes low. If the FIFO is not empty, *IRQ will go low TINAIRQL ns after *INTACK returns high.

After *INTACK goes low, the NHI-ET waits TPR ns to allow for the propagation of *INTPO and *INTPI through the daisy chain.

The minimum propagation time, TPR, through the daisy chain can be extended by delaying the *HRD signal by any amount, TPRE.

If the falling edge of *HRD occurs less than TPR ns after *INTACK, ITACK starts TPR ns after *INTACK, otherwise, ITACK starts after the falling edge of *HRD.

11.1.0 TIMING PARAMETER TABLES

11.1.1 HOST READ, WRITE, and READ-MODIFY-WRITE TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TADS	ADDRESS SETUP TIME	0	-	ns
TADH	ADDRESS HOLD TIME	200	-	ns
THCSCL	HCS_L LOW TO COMMAND LOW	0	-	ns
TACKWH	DATA ACKNOWLEDGE LOW TO WRITE HIGH	0	-	ns
TWASH	HWRL_L, HWRH_L HIGH TO HCS_L HIGH	0	-	ns
TACKH	END OF CYCLE TO DATA ACKNOWLEDGE HIGH	0	30	ns
TACKL(1)	NO CONTENTION	0	500	ns
TACKL(2)	WITH CONTENTION	0	800	ns
TACKL(3)	WORST CASE, ONCE AT START OF MESSAGE	0	2.8	us
TDS	DATA SETUP TIME	0	-	ns
TDH	DATA HOLD TIME	0	-	ns
TACKRH	DATA ACKNOWLEDGE LOW TO READ HIGH	0	-	ns
TRDLZ	HRD_L LOW TO DATA LOW Z	0	20	ns
TRDHDHZ	HRD_L HIGH TO DATA HIGH Z	0	30	ns
TRDHWL	HRD_L HIGH TO WRITE LOW	30	-	ns

11.1.2 I/O READ and TERMINAL ADDRESS READ TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TVARL	VALID ADDRESS TO I/O_RD_L LOW	50	-	ns
TRHVA	ADDRESS VALID AFTER I/O_RD_L HIGH	50	-	ns
TIORW	I/O_RD_L PULSE WIDTH	190	210	ns
TRHDHZ	I/O_RD_L HIGH TO DATA HIGH Z	0	200	ns
TRHCML	I/O_RD_L HIGH TO CMDS LOW	100	-	ns
TCMHRL	CMDS HIGH TO I/O_RD_L LOW	100	-	ns
TIODHZDL	I/O DATA BUS HIGH Z TO DATA ON BUS	100	-	ns
TRLDS	I/O_RD_L LOW TO DATA STABLE	-	80	ns

11.1.3 I/O WRITE and COMMAND WRITE TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TVAWL	VALID ADDRESS TO I/O_WR_L LOW	50	-	ns
TWHVA	ADDRESS VALID AFTER I/O_WR_L HIGH	50	-	ns
TIOWW	I/O_WR_L PULSE WIDTH	90	110	ns
TDS	DATA SETUP TIME	25	50	ns
TDH	DATA HOLD TIME	40	80	ns
TCMWW	COMMAND WRITE PULSE WIDTH	290	310	ns
TCMHWL	COMMAND STROBE HIGH TO I/O_WR_L LOW	40	-	ns
TWHCML	I/O_WR_L HIGH TO CMDS LOW	100	-	ns

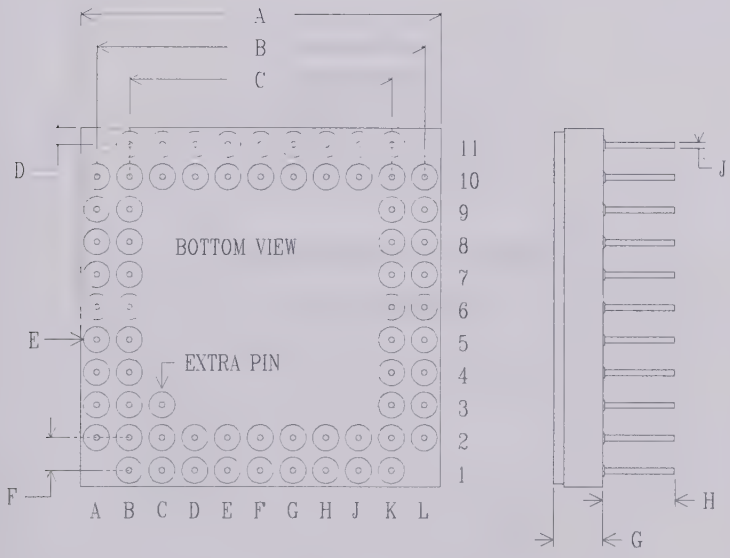
11.1.4 INTERRUPT ACKNOWLEDGE CYCLE TABLE

SYMBOL	PARAMETER	MIN	MAX	T
TIRQPOH	IRQ_L LOW TO INTPO HIGH	-	20	ns
TPILPOL	INTPI_L LOW TO INTPO_L LOW	-	40	ns
TPIHPOH	INTPI_L HIGH TO INTPO_L HIGH	-	40	ns
TINAIRQH	INTACK_L LOW TO IRQ_L HIGH	0	200	ns
TINAIRQL	INTACK_L HIGH TO NEXT IRQ_L LOW	0	200	ns
TRINAH	HRD_L HIGH TO INTACK_L HIGH	0	-	ns
ITACK	HRD_L LOW TO DTACK_L LOW	300	400	ns
TACKRH	DTACK_L LOW TO HRD_L HIGH	0	-	ns
TRDLZ	HRD_L LOW TO DATA IN LOW Z	0	20	ns
TRDHDHZ	HRD_L HIGH TO DATA IN HIGH Z	0	30	ns
TACKH	END OF CYCLE TO *DTACK HIGH	0	30	ns
TIRQPOL	IRQ_L HIGH TO INTPO LOW	10	20	ns
TINARL	INTACK_L LOW TO HRD_L LOW	0	30	ns

12.0.0 PIN FUNCTIONS AND MECHANICAL DRAWINGS

12.0.1 NHI-1582ET- 69 PGA

Pin	Function	Pin	Function	Pin	Function	Pin	Function
A2	H_ADR7	B9	H_DAT8	F2	PLSCMD/B_JAM	K3	H_ADR14
A3	H_ADR8	B10	H_DAT9	F10	H_DAT15	K4	TXINH_B
A4	H_ADR10	B11	H_DAT10	F11	HWRH_L	K5	+5V
A5	H_ADR12	C1	H_ADR5	G1	H_DAT12	K6	INTACK_L
A6	H_DAT1	C2	BUS_A_L	G2	TXINH_A	K7	DSC_INTPO_L
A7	H_DAT2	C3	H_ADR13	G10	RST_L	K8	I/O_ADR1
A8	H_DAT4	C10	H_ADR1	G11	HCS_L	K9	I/O_DAT5
A9	H_DAT5	C11	H_DAT11	H1	BUS_B_L	K10	I/O_DAT4
A10	H_DAT6	D1	H_ADR3	H2	I/O_WR_L	K11	I/O_DAT0
B1	H_ADR6	D2	H_ADR4	H10	I/O_DAT2	L2	NC
B2	GND	D10	H_DAT13	H11	SSF_TF	L3	CMDS
B3	BUS_A	D11	HRD_L	J1	GND	L4	I/O_RD_L
B4	H_ADR9	E1	DTACK_L	J2	BUS_B	L5	+5V
B5	H_ADR11	E2	H_ADR2	J10	I/O_DAT3	L6	INTPI_L
B6	H_DAT0	E10	H_DAT14	J11	CLK	L7	I/O_ADR2
B7	H_DAT3	E11	HWRL_L	K1	GND	L8	I/O_DAT7
B8	H_DAT7	F1	IRQ_L	K2	MDCDRST	L9	I/O_DAT6
						L10	I/O_DAT1



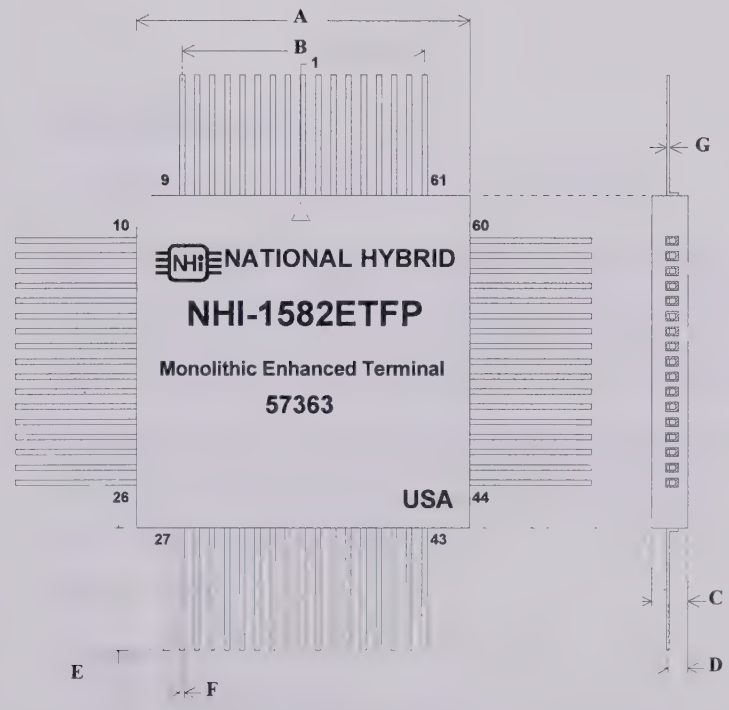
TOP VIEW

DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ.	0.010
B	10 EQ. SP. @ 0.100 = 1.000	
C	0.800	0.010
D	0.050	TYP
E	0.065 DIA	TYP
F	0.100	TYP
G	0.150	MAX
H	0.220	MIN
J	0.018 DIA.	0.002

NHI-1582ET 69 PGA Package Detail

12.0.2 NHI-1582ETFP- 68 QUAD FLAT PACK

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	I/O_DAT1	18	BUS_A	35	H_ADR4	52	H_DAT3
2	I/O_DAT2	19	BUS_A_L	36	H_ADR5	53	H_DAT4
3	I/O_DAT3	20	H_ADR13	37	H_ADR6	54	H_DAT5
4	I/O_DAT4	21	CMDS	38	H_ADR7	55	H_DAT6
5	I/O_DAT5	22	TXINH_B	39	+5V	56	H_DAT7
6	I/O_DAT6	23	BUS_B	40	+5V	57	H_DAT8
7	I/O_DAT7	24	BUS_B_L	41	GND	58	H_DAT9
8	HCS_L	25	H_ADR14	42	GND	59	H_DAT10
9	SSF_TF	26	I/O_RD_L	43	GND	60	H_DAT11
10	RST_L	27	I/O_WR_L	44	H_ADR8	61	H_ADR1
11	CLK10	28	MDCDRST	45	H_ADR9	62	HRD_L
12	I/O_ADR1	29	PLSCMD/B_JAM	46	H_ADR10	63	HWRL_L
13	I/O_ADR2	30	IRQ_L	47	H_ADR11	64	HWRH_L
14	DSC_INTPO_L	31	DTACK_L	48	H_ADR12	65	H_DAT13
15	INTPI_L	32	H_DAT12	49	H_DAT0	66	H_DAT14
16	INTACK_L	33	H_ADR2	50	H_DAT1	67	H_DAT15
17	TXINH_A	34	H_ADR3	51	H_DAT2	68	I/O_DAT0



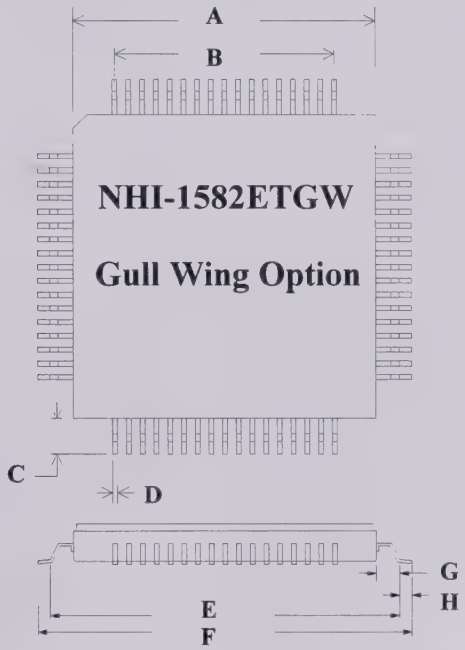
DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ	0.010
B	16 EQ SP @	0.050 = 0.800
C	0.140	MAX
D	0.065	0.010
E	0.400	MIN
F	0.018	0.002
G	0.010	0.002

NHI-1582ETFP 68 Pin Quad Flat Package Detail and Marking

12.0.3 NHI-1582ETGW- 68 QUAD GULL WING Lead Formed Flat Pack

NHI-1582ETGW
Gull Wing Option

DIM	TYP (inches)	TOL (+/- inches)
A	1.100 SQ	0.010
B	16 EQ SP @	0.050 = 0.800
C	0.130	TYP
D	0.018	0.002
E	1.270	MIN
F	1.360	0.015
G	0.085	REF
H	0.045	0.010



14.0.0 APPLICATION NOTES

15.0.0 NHI-15182EMT(Extended Memory Terminal) ADDENDUM

The NHI-15182EMT is a low cost complete interface between a dual redundant MIL-Std-1553 bus and a host processor. The device has all the features of the popular NHI-1582ET and functions as a programmable Bus Controller, Remote Terminal, and Bus Monitor containing a protocol chip, two +5V monolithic transceivers, and the extended 64K words of SRAM. The unit is available packaged in a 1.1" x 1.1" 128 pin ceramic quad flatpack. The only external components required are two coupling transformers.

The NHI-15182EMT appears to the host computer as 64K words of 16 bit wide memory controlled by standard RAM signals. The device can thus be easily interfaced with all popular processors and buses. Multiple Mode Memory Maps provide virtually unlimited capability for all Bus Controller, Bus Monitor and Concurrent RT/Monitor applications.

15.0.1 EMT Features:

Complies With:

MIL-STD-1553A
MIL-STD-1553B Notices I and II
MIL-STD-1760B
MacAir MDC A3818
EFA/STANAG-3838 requirements for Eurofighter Aircraft

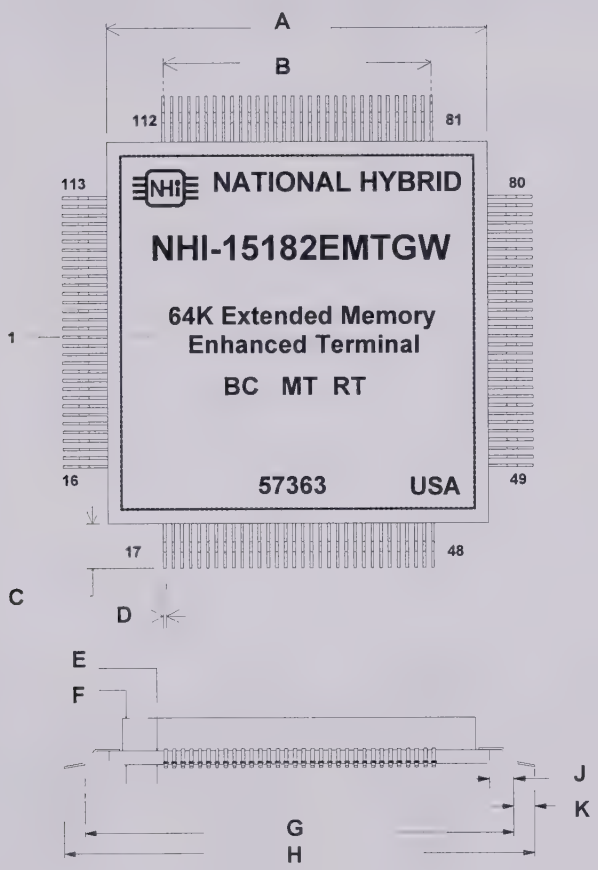
- Appears to host as a Dual Port Double Buffered 64K x 16 SRAM
- Low total power consumption.

- Footprint less than 1.25 square inches
- External Time Tag Clock Input
- Address Latch Input Pin
- 16 Bit I/O Data Bus
- 14 Pulse Command Output Pins
- Disconnect Output Line (Mil-Std-1760 Feature)
- Sync Without Data Mode Code Pulse Output Pin.

15.0.2 NHI-15182EMT 128 QFP Pin Functions

Pin	Function	Pin	Function	Pin	Function	Pin	Function
1	BUS_A_L	33	H_DAT2	65	RAMDTA_3 IOD_03	97	I/O_RD_L
2	BUS_A_L	34	H_DAT3	66	IOA_14 / MADR_14	98	IOD_12 / MADR_10
3	BUS_A_L	35	DBCA_L	67	ADR_LAT_L	99	IOD_13 / MADR_11
4	TRAN_PWR	36	H_DAT4	68	RAMDTA_4 / IOD_04	100	IOD_14 / MADR_12
5	TRAN_PWR	37	H_DAT5	69	RAMDTA_5 IOD_05	101	DSC_INTPO_L
6	TRAN_PWR	38	PLSOUT_01_H	70	IOA_15 / MADR_15	102	INTPI_L
7	TXINH_A	39	H_DAT6	71	RAMDTA_6 / IOD_06	103	INTACK_L
8	TRAN_PWR	40	H_DAT7	72	RAMDTA_7 / IOD_07	104	I/O_WR_L
9	TRAN_PWR	41	PLSOUT_02_H	73	IOA_16 / MADR_16	105	PLSOUT_07_H
10	BUS_A	42	H_DAT8	74	MRDO_L	106	CMDS
11	BUS_A	43	H_DAT9	75	MWR_L	107	PLSOUT_08_H
12	BUS_A	44	H_DAT10	76	DISCN_H	108	PLSOUT_09_H
13	DTACK_L	45	H_DAT11	77	HCS_L	109	PLSOUT_10_H
14	H_DAT12	46	PLSOUT_03_H	78	SSF_TF	110	IRQ_L
15	H_ADR2	47	H_ADR1	79	RST_L	111	PLSOUT_11_H
16	H_ADR3	48	HRD_L	80	CLK_H	112	No_Connect
17	PLSOUT_12_H	49	HWRL_L	81	IOD_15 / MADR_00	113	BUS_B_L
18	H_ADR4	50	PLSOUT_04_H	82	IOA_01 / MADR_01	114	BUS_B_L
19	H_ADR5	51	HWRH_L	83	H_ADR13	115	BUS_B_L
20	PLSOUT_13_H	52	H_DAT13	84	IOA_02 / MADR_02	116	TRAN_GND
21	H_ADR6	53	H_DAT14	85	EXT_TMTG	117	TRAN_GND
22	H_ADR7	54	H_DAT15	86	IOA_03 / MADR_03	118	TRAN_GND
23	H_ADR8	55	DIG_PWR	87	H_ADR14	119	TXINH_B
24	H_ADR15	56	DIG_PWR	88	IOA_04 / MADR_04	120	TRAN_GND
25	H_ADR9	57	DIG_GND	89	IOA_05 / MADR_05	121	TRAN_GND
26	H_ADR10	58	DIG_GND	90	MCD_01_PLS_H	122	BUS_B
27	H_ADR16	59	RAMDTA_0 IOD_00	91	IOD_08 / MADR_06	123	BUS_B
28	H_ADR11	60	PLSOUT_05_H	92	PLSCMD / B_JAM	124	BUS_B
29	H_ADR12	61	RAMDTA_1 IOD_01	93	IOD_09 / MADR_07	125	TRAN_GND
30	H_DAT0	62	PLSOUT_06_H	94	MDCDRST	126	TRAN_GND
31	H_DAT1	63	RAMDTA_2 IOD_02	95	IOD_10 / MADR_08	127	TRAN_PWR
32	EXT_MCS_L	64	IOA_13 MADR_13	96	IOD_11 / MADR_09	128	TRAN_PWR

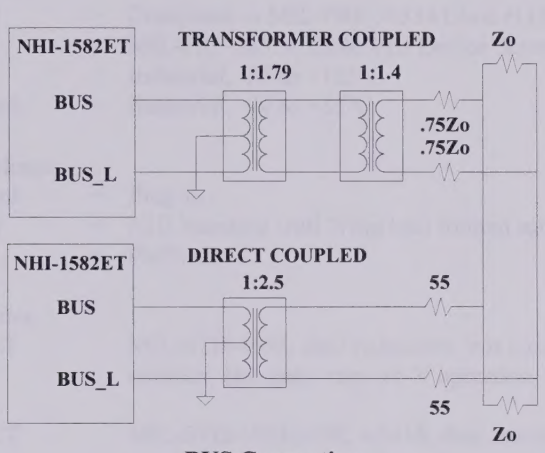
15.0.3 NHI-15182EMT 128 QFP Mechanical Drawing



DIM	Typ (inches)	TOL (+/- inches)
A	1.100	0.005
B	31 EQ SP @ 0.025	
C	0.130	TYP
D	0.010	0.002
E	0.040	0.005
F	0.140	0.010
G	1.270	MIN
H	1.270	0.015
J	0.085	REF
K	0.045	0.010

16.0.0 MATING TRANSFORMER REFERENCE

The NHI-1582ET series requires a transformer with a turns ratio of 1:2.5 for Direct Coupling, and a turns ratio of 1:1.79 for Transformer Coupling to the Mil-Std-1553 Bus. Technitrol part number Q1553-45 or equivalent is recommended. The center tap on the transceiver side of the isolation transformer must be grounded.



BUS Connections

Device	Power Supply +V	Turns Ratio Direct	Turns Ratio Stub	Technitrol Part Number	DESC SMD
NHI-1582ET	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9555801
NHI-1583ET	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9555802
NHI-1598ET	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9555803
NHI-1599ET	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9555804
NHI-15103ET	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9555805
NHI-15104ET	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	5962-9555806
NHI-15182EMT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	
NHI-15183EMT	+5V Only	1.00:2.50	1.00:1.79	Q1553-45	

17.0.0 Ordering Information

NHI-1582ETGW/883

Grade

883	=	Compliant to MIL-PRF-38534 Class H (Mil-Std-883 Test Methods)
M	=	MIL-PRF-38534 Table VIII Device Screening, -55 to +125°C
T	=	Industrial, -55 to +125°C
Blank	=	Industrial, -40 to +85°C

Package

Blank	=	Plug-In
GW	=	NHI Standard Gull Wing lead formed surface mount flatpack
FP	=	FlatPack

Device

82ET	MIL-STD-1553, dual redundant, bus controller, remote terminal, bus monitor, 16k static ram, +5 V operation, monolithic transceivers.
83ET	MIL-STD-1553/MDC A3818, dual redundant, bus controller, remote terminal, bus monitor, 16k static ram, +5 V operation, monolithic transceivers.
98ET	MIL-STD-1553, dual redundant, bus controller, remote terminal, bus monitor, 16k static ram, +5 V operation, monolithic transceivers, external time tag clock input.
99ET	MIL-STD-1553/MDC A3818, dual redundant, bus controller, remote terminal, bus monitor, 16k static ram, +5 V operation, monolithic transceivers, external time tag clock input.
103ET	MIL-STD-1553, dual redundant, bus controller, remote terminal, bus monitor, 16k static ram, +5 V operation, monolithic transceivers, address latch input pin.
104ET	MIL-STD-1553/MDC A3818, dual redundant, bus controller, remote terminal, bus monitor, 16k static ram, +5 V operation, monolithic transceivers, address latch input pin.
182EMT	MIL-STD-1553, dual redundant, bus controller, remote terminal, bus monitor, 64k static ram, +5 V operation, monolithic transceivers.
183EMT	MIL-STD-1553/MDC A3818, dual redundant, bus controller, remote terminal, bus monitor, 64k static ram, +5 V operation, monolithic transceivers.

**SMD Listing: DESC Drawing# 5962-95558
See QML-38534 for NHI's Qualification under Mil-PRF-38534